P.E.S. COLLEGE OF ENGINEERING, MANDYA

(An Autonomous Institution affiliated to VTU, Belagavi)

MASTER OF TECHNOLOGY
In
VLSI Design and Embedded System

SCHEME AND SYLLABUS

2022– 23

Department of Electronics and Communication Engineering

P.E.S COLLEGE OF ENGINEERING, MANDYA-571401

KARNATAKA

Vision

PESCE shall be a Leading Institution Imparting Quality Engineering and Management Education developing creative and socially responsible professionals.

Mission

- Provide state of the art infrastructure, motivate the faculty to be proficient in their field of Specialization and adopt best teaching-learning practices.
- Impart engineering and managerial skills through competent and committed faculty using Outcome based educational curriculum.
- Inculcate professional ethics, leadership qualities and entrepreneurial skills to meet the societal needs.
- Promote research, product development and industry-institution interaction.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

About the Department:

The department of Electronics and Communication Engineering was incepted in the year 1967 with an undergraduate program in Electronics and Communication Engineering. Initially program had an intake of 60 students and presently 150 students graduate every year. The long journey of 50 years has seen satisfactory contributions to the society, nation and world. The alumni of this department have strong global presence making their alma mater proud in every sector they represent.

Department has started its PG program in the year 2012 in the specialization of VLSI design and Embedded systems. Equipped with qualified and dedicated faculty department has focus on VLSI design, Embedded systems and Image processing. The quality of teaching and training has yielded high growth rate of placement at various organizations. Large number of candidates pursuing research programs (M.Sc/Ph D) is a true testimonial to the research potential of the department.

Vision

The department of E & C would Endeavour to create a pool of Engineers who would be **extremely competent technically, ethically strong** also fulfil their obligation in terms of **social responsibility**.

Mission

- **M1:** Adopt the best pedagogical methods and provide the best facility, infrastructure and an ambience conducive to imbibe technical knowledge and practicing ethics.
- **M2**:Group and individual exercises to inculcate habit of analytical and strategic thinking to help the students to develop creative thinking and instill team skills
- **M3**:MoUs and Sponsored projects with industry and R & D organizations for Collaborative learning.
- **M4**: Enabling and encouraging students for continuing education and moulding them for life-long learning process.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(A) Programme Learning Objectives (PLOs)

M.Tech in VLSI Design and Embedded system during two years term, aims to

1. Provide the students with strong fundamental and advanced knowledge in VLSI design and Embedded system with an emphasis to solve engineering problems.
2. Train the students in VLSI and Embedded system design tools and make them fit for the industries.
3. Inculcate in students the professional and ethical attitude, effective Communication skills, team spirit and nurture them as leaders.
4. Provide teaching skills and inculcate spirit of research.
5. Motivate to continue education leading to doctoral degree and choose research as Career option.

(B) Programme Outcomes (POs):

The Master of Technology Programme in Electronics and Communication Engineering [M.Tech in VLSI Design and Embedded systems] must demonstrate that its Post graduates have

1. An ability to apply knowledge gained out of this program to develop products and solutions in the area of VLSI design and Embedded Systems.
2. An understanding of professional and ethical responsibilities at national and internationallevels.
3. An ability to effectively communicate both written and oral on social and technical Problems at national and global scenarios.
4. An ability to engage in independent and lifelong learning in the broad context of Technological change.
5. Ability to carry- out independent research.

A total of 80 credits for 2 years M.Tech programme

Credit pattern

Professional Core Courses: - I Semester 08 credits

II Semester 05 credits

III Semester 04 credits

Total credits **for Professional core courses** is **17** credits

Integrated Professional Core Courses: - I Semester 04 credits

II Semester 04 credits

Total credits for **Integrated Professional core courses** is **08** credits

Professional Elective Course: - I Semester 06 credits

II Semester 06 credits

III Semester 03 credits

Total credits for **Professional Elective courses** is **15** credits

Open Elective course:03 credits

Self Study course: - 02 credits

Societal Project: - 02 credits

Lab: - 04 credits

Internship: - 06 credits

Pedagogy Training: - 03 credits

Term Paper:- 02 credits

Project work:- 18 credits,

A total of 80 credits for 2 years M.Tech programme

I – Semester									
Sl. No.	**Course Code**	**Course Title**	**Teaching Hours/Week**			**Examination Marks**			**Credits**
			Theory	**Tutorial**	**Practical / Field work**	**CIE**	**SEE**	**Total**	
1.	P22MECE11	CMOS VLSI Design (PCC)	04	--	--	50	50	100	4
2.	P22MECE12	Embedded system design (PCC)	04	--	--	50	50	100	4
3.	P22MECE13	Digital System design using Verilog(IPCC)	03	--	02	50	50	100	4
4.	P22MECE14X	Professional Elective – I (PEC)	03	--	--	50	50	100	3
5.	P22MECE15X	Professional Elective – II (PEC)	03	--	--	50	50	100	3
6.	P22MECEL16	VLSI Design and Embedded system –I (PCCL)	01	--	02	50	50	100	2
Total			**18**	**--**	**04**	**300**	**300**	**600**	**20**

Professional Elective - I			**Professional Elective - II**		
Sl. No	**Course Code**	**Course Title**	**Sl. No**	**Course Code**	**Course Title**
1.	P22 MECE141	Advances In IC Fabrication Technology	1.	P22MECE151	ASIC Design
2.	P22MECE142	Physical Design	2.	P22MECE152	MEMS and Sensors
3.	P22MECE143	System on Chip	3.	P22MECE153	Applications of Machine learning in VLSI
4.	P22MECE144	Internet of things	4.	P22MECE154	Hardware-Software Co-design

Note: PCC: Professional Core Course | IPCC-Integrated Professional Core Courses | PEC-Professional Elective Course|

PCCL - Professional Core Course Laboratory | MCC – Mandatory Credit Course

II – Semester									
Sl. No.	**Course Code**	**Course Title**	**Teaching Hours/Week**			**Examination Marks**			**Credits**
			Theory	**Tutorial**	**Practical / Field work**	**CIE**	**SEE**	**Total**	
1.	P22MECE21	Research Methodology and IPR (MCC) [Common to all PG Programs]	03	--	--	50	50	100	3
2.	P22MECE22	System Verilog (IPCC)	04	--	02	50	50	100	5
3.	P22MECE23	CMOS Mixed Mode VLSI Circuits (PCC)	04	--	--	50	50	100	4
4.	P22MECE24X	Professional Elective – III (PEC)	03	--	--	50	50	100	3
5.	P22MECE25X	Professional Elective – IV (PEC)	03	--	--	50	50	100	3
6.	P22MECEL26	VLSI Design and Embedded system -II (PCCL)	01	--	02	50	50	100	2
Total			**18**	**--**	**04**	**300**	**300**	**600**	**20**

Professional Elective - III			**Professional Elective - IV**		
Sl. No	**Course Code**	**Course Title**	**Sl. No**	**Course Code**	**Course Title**
1.	P22MECE241	ARM Processors	1.	P22MECE251	Low power VLSI design
2.	P22MECE242	Embedded system design with FPGA	2.	P22MECE252	Automotive Electronics
3.	P22MECE243	Robotics and Automation	3.	P22MECE253	Design of VLSI system
4.	P22MECE244	Advanced in VLSI system	4.	P22MECE254	RF Integrated Circuits

Note: PCC: Professional Core Course | IPCC-Integrated Professional Core Courses | PEC-Professional Elective Course|

PCCL - Professional Core Course Laboratory | MCC – Mandatory Credit Course

III – Semester									
Sl. No.	**Course Code**	**Course Title**	**Teaching Hours/Week**			**Examination Marks**			**Credits**
			Theory	**Tutorial**	**Practical / Field work**	**CIE**	**SEE**	**Total**	
1.	P22MECE31	Multi core architecture and Programming (PCC)	04	--	--	50	50	100	4
2.	P22MECE32X	Professional Elective – V(PEC)	03	--	--	50	50	100	3
3.	P22MECEO33X	Open Elective Course (OEC)	03	--	--	50	50	100	3
4.	P22MECE34	Societal Project	--	--	04	100	--	100	2
5.	P22MECE35	Self-Study Course – I (AEC)	--	--	--	100	--	100	2
6.	P22MECE36	Project Phase – I	-	--	04	100	--	100	2
7.	P22MECE37	Internship	*(06 weeks Internship Completed during the intervening vacation of II and III semesters)*			50	50	100	6
Total			**10**	**--**	**08**	**500**	**200**	**700**	**22**

Professional Elective - V			Open Elective		
Sl. No	**Course Code**	**Course Title**	**Sl. No**	**Course Code**	**Course Title**
1.	P22MECE321	High Performance digital VLSI Circuit Design	1.	P22MECEO331	Embedded systems
2.	P22MECE322	Network on chip	2.	P22MECEO332	Microcontrollers
3.	P22MECE323	Real time Operating system	3.	P22MECEO333	Automotive Electronics
4.	P22MECE324	VLSI Testing and Verification	4.	P22MECEO334	Future Technology

Note: PCC: Professional Core Course | IPCC-Integrated Professional Core Courses | PEC-Professional Elective Course |

OEC – Open Elective Course | AEC – Ability Enhancement Course

IV – Semester									
Sl. No.	Course Code	Course Title	Teaching Hours/Week			Examination Marks			Credits
			Theory	Tutorial	Practical / Field work	CIE	SEE	Total	
1.	P20MECE41	Project Phase – II	--	--	08	100	100	200	16
2.	P20MECE42	Term Paper	--	--	--	100	--	100	2
Total			**--**	**--**	**--**	**200**	**100**	**300**	**18**

Category of Courses:

Integrated Professional Core Course (IPCC)

Integrated Professional Core Course (IPCC) refers to Professional Theory Core Course Integratedwith practical of the same course. The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated byonly CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper.

Ability Enhancement Courses (AEC):

- These courses are prescribed to help students to enhance their skills in fields connected to the field of specialisation as well allied fields that leads to employable skills. Involving in learning such courses are impetus to lifelong learning.
- The courses under this category are online courses published in advance and approved by the concerned Board of Studies.
- Registration to Ability Enhancement Course shall be done in consultation with the mentor and is compulsory during the concerned semester.
- In case a candidate fails to appear for the proctored examination or fails to pass the selected online course, he/she can register and appear for the same course if offered during the next session or register for a new course offered during that session, in consultation with the mentor.

The Self-Study Course is an AEC and should be chosen from the available 08 weeks NPTEL online courses recommended by the concerned Board of Studies. The student can undergo NPTEL course registration during I / II / III Semester and the credit will be considered in III Semester. The 100 marks CIE assessment is based on the final NPTEL score (i.e. Online assignments: 25% + Proctored exam: 75%). The NPTEL score will be mapped directly to the CIE marks only if he /she has completed the NPTEL course (i.e. Certification). Those, who do not take-up/ Complete the NPTEL course shall be declared as failed and have to complete during the subsequent examination after satisfying the NPTEL requirements.

Societal Project

Students in consultation with the internal guide as well as with external guide (much preferable) shall involve in applying technology to work out/proposing viable solutions for societal problems. CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.

Those, who have not pursued /completed the Societal Project, shall be declared as fail in the course and have to complete the same during subsequent semester/s after satisfying the Societal Project requirements. There is no SEE for this course.

Internship

All the students shall have to undergo a mandatory internship of **06 weeks** during the vacation of II and III semesters. A Semester End Examination shall be conducted during III semester and the prescribed internship credit shall be counted in the same semester. The internship shall be considered as a head of passing and shall be considered for vertical progression as well as for the award of degree. Those, who do not take-up/complete the internship shall be declared as fail in the internship course and have to complete the same during the subsequent Semester End examination after satisfying the internship requirements.

Internship SEE shall be as per the University norms. CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded for Internship shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.

Project Work Phase-1

The project work shall be carried out individually. However, in case a disciplinary or interdisciplinary project requires more participants, then a group consisting of not more than three shall be permitted. Students in consultation with the guide/co-guide (if any) in disciplinary project or guides/co-guides (if any) of all departments in case of multidisciplinary projects, shall pursue a literature survey and complete the preliminary requirements of the selected Project work. Each student shall prepare a relevant introductory project document, and present a seminar.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, all Guide/s and co-guide/s (if any) and a senior faculty of the concerned departments. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill, and performance in the Question and Answer session in the ratio of 50:25:25.

Project Work Phase-2

Students in consultation with the guide/co-guide (if any) in disciplinary project or guides/co-guides (if any) of all departments in case of multidisciplinary projects, shall continue to work of Project Work phase -1to complete the Project work. Each student / batch of students shall prepare project document and present a seminar.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, all Guide/s and co-guide/s (if any) and a senior faculty of the concerned departments. The CIE marks awarded for project work phase -1, shall be based on the ***overall completion & demonstration / execution of the project work***, ***Project Presentation skill and performance in the Question and Answer session*** in the ratio of 50:25:25.

SEE evaluation shall be for 100 marks and it is based on ***Thesis Report (Average Score of External and Internal Examiner)*** and ***project viva voce*** in the ratio of 50:50 that has to be conducted jointly by internal and external examiner.

Term Paper

The term paper is purely based on the project work he/she chooses. The Term paper shall be for 100 marks CIE only. It has to be evaluated by the committee formed by HOD consisting of PG coordinator, guide and subject expert internal/ external for each candidate.

The term paper evaluation is based on the publication of an article in peer reviewed conference/ journal (national/ international) and quality of the journal. If the term paper is not published by the candidate or the same is communicated for publication at the end of his/ her tenure, then the committee formed by HOD consisting of PG coordinator, guide and subject expert internal/ external for each candidate will assess for the award of credit.

CMOS VLSI Design

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – I

Course Code:	**P22MECE11**	**Credits:**	**04**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Provide the basic knowledge of MOSFETs.
- Explain the MOS Transistor threshold voltage equation.
- Describe the second order effects.
- Provides the knowledge of lambda based design rule and process technology.
- Outline the concepts of Basics of Digital CMOS Design.
- Discuss the concepts of clocking in digital CMOS design.
- Describe the different types of semiconductor memories.

UNIT – I	**8 Hours**

MOS Transistor Theory: Introduction, Long-Channel I-V Characteristics, C-V Characteristics, Non ideal I-V Effects, Mobility Degradation and Velocity Saturation, Channel Length Modulation, Threshold Voltage Effects, Leakage, DC Transfer Characteristics, Static CMOS Inverter DC Characteristics, Beta Ratio Effects, Noise Margin, Pass Transistor DC Characteristics.

CMOS Processing Technology: Introduction, CMOS Technologies, Wafer Formation, Photolithography, Well and Channel Formation, Silicon Dioxide (SiO2), Isolation, Gate Oxide, Gate and Source/Drain Formations, Contacts and Metallization, Passivation, Metrology, Layout Design Rules, Design Rule Background.

Text 1: Chapter 2.1 - 2.3, 2.4-(2.4.1,-2.4.4), 2.5 Chapter 3.1, 3.2, 3.3.1

Self-Study Component:	1. Study on Temperature dependence, Geometry Dependence, Layout Design Rule.

UNIT – II	**8 Hours**

CMOS Process Enhancements: Transistors, Interconnect, Circuit Elements, Beyond Conventional CMOS, Technology-Related CAD Issues: Design Rule Checking (DRC), Circuit Extraction, Manufacturing Issues: Antenna Rules, Layer Density Rules, Resolution Enhancement Rules, Metal Slotting Rules, Yield Enhancement Guidelines.

Delay: Introduction, Transient Response, RC Delay Model, Logical Effort of Paths-Delay in Multistage logic Networks, Choosing The Best Number Of Stages, Example .

Power: Introduction, Dynamic Power-Activity factor, Capacitance, Voltage, Static Power-Sources, Power Gating.

Text1: Chapter 3.4 – 3.6, Chapter 4.1 - 4.3, 4.5-(4.5.1-4.5.3), Chapter 5.1, 5.2-(5.2.1-5.2.3) 5.3-(5.3.1,5.3.2).

Self-Study Component:	1. Analyse and present Linear Delay Model, Timing Analysis Delay Models, Energy-Delay Optimization

UNIT – III	**8 Hours**

Circuit Simulation: Introduction, A SPICE Tutorial-source and Passive Component, Transistor DC Analysis, Inverter Transient Analysis, Sub Circuits and Measurement, Optimization, Other HSPICE Commands, Device Models-level1,2,3 Models, BSIM models, Diffusion Capacitance Models, Design Corners, Device Characterization-IV Characteristics, Threshold Voltage, Gate Capacitance.

Combinational Circuit Design: Introduction, Circuit Families-static CMOS, Ratioed

Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Pass Transistor Circuits, Circuit Pitfalls-Threshold Drops, Ratio Failure, Leakage, Charge Sharing, Power Supply Noise, Hotspots.

Text1: Chapter 8.1–8.3, 8.4-(8.4.1-8.4.3) Chapter 9.19.2 [9.2.1(9.2.1.1, 9.2.1.2), 9.2.2, 9.2.3, 9.2.4 (9.2.4.1, 9.2.4.2), 9.2.5] , 9.3-(9.3.1-9.3.6).

Self-Study Component:	1. Create a Circuit Characterization. 2. Study on Interconnect Simulation.

UNIT – IV	**8 Hours**

Sequential Circuit Design: Introduction, Sequencing Static Circuits-Sequencing Methods, Max and Min Delay Constraints, Circuit Design of Latches and Flip-Flops-Conventional CMOS Latches and Flip Flops, Pulsed Latches, Resettable Latches, Enabled Latches and Flip flops, Static Sequencing Element Methodology-Choice of Elements, Characterizing Sequencing Element Delays, State Retention Registers.

Datapath Subsystems: Introduction, Addition/Subtraction-Single Bit Addition, Carry Propagate Addition –Carry Ripple Adder, Carry Generation and Propagation, PG Carry Ripple Carry Skip and Carry Look-ahead Adder , Subtraction, Multiple Input Addition.

Text1:Chapter 10.1,10.2(10.2.1-10.2.3),10.3(10.3.1-10.3.5),10.4(10.4.1-10.4.3),
Chapter 11.1, 11.2.1, 11.2.2 -(11.2.2.1-11.2.2.6),11.2.3,11.2.4.

Self-Study Component:	1. Study and present on Sequencing Dynamic Circuits, Synchronizers, One/Zero Detectors & Comparators.

UNIT – V	**8 Hours**

Datapath subsystem: Counters-Binary counters, Fast Binary Counters, Ring and Johnson Counter, Linear Feedback Shift Registers., Boolean Logical Operations, Coding-Parity, Error Correcting Codes, Gray Code, XOR/XNOR Circuit Forms, Shifters-Funnel and Barrel Shifter, Alternative Shift Function.

A**rray Subsystems:** Introduction, SRAM-SRAM Cells, Row and Column Circuitry, multiported SRAM and register Files, Large SRAMs and Low Power SRAMs, Area, Delay and Power of RAMs and Register files.

Text1:Chapter 11.5 – 11.8, Chapter 12.1 – 12.2

Self-Study Component:	1. Study of Multiplication. 2. Explore and analyze DRAM.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Apply** the knowledge of the basic VLSI circuit to interpret the concept of MOS Theory and CMOS Processing Technology.	L2	PO1 [L2]
CO2	**Analyze** the different techniques in designing Combinational and Sequential CMOS circuits.	L2, L3	PO1 [L2], PO4 [L3]
CO3	**Analyze** the Data path and Array path subsystems in Digital Circuits.	L2, L3	PO1 [L2] PO5 [L3]
CO4	**Illustrate** and **outline** concept of delay and power in CMOS Circuits.	L2, L3	PO1 [L2] PO4 [L3]
CO5	**Design** and Simulate the MOSFET	L3	PO4 [L3]

	devices using CAD tools.		PO5 [L3]

Text Book(s):

1. Neil H. E. Weste, David Money Harris, "**CMOS VLSI Design: a Circuits and Systems Perspective"**, Pearson(Fourth Edition),ISBN 10: 0-321-54774-8, ISBN 13: 978-0-321-54774-3

Reference Book(s):

1. Sung Mo Kang &Yosuf Lederabic Law, "**CMOS Digital Integrated Circuits: Analysis and Design**", McGraw-Hill (Third Edition), ISBN: 9780071243421, 9780071243421.
2. Wayne, Wolf, "**Modern VLSI design: System on Silicon**", Pearson Education", 2nd Edition, ISBN: 81-7758-411-1.
3. Douglas A Pucknell & Kamran Eshragian, "**Basic VLSI Design**", PHI 3rd Edition (original Edition – 1994), ISBN: 978-81-203-0986-9.
4. John .P. Uyemura, "**Introduction to VLSI Circuits and Systems**", John Wiley.

Web and Video link(s):

1. https://www.youtube.com/watch?v=oL8SKNxEaHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM.

E-Books/Resources:

1. https://books.google.co.in/books/about/CMOS_VLSI_Design_A_circuits_and_systems.html?id=0RAwDwAAQBAJ&redir_esc=y.
2. https://pages.hmc.edu/harris/cmosvlsi/4e/index.html.

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2	2			2	
#3	2				2
#4	3			2	

EMBEDDED SYSTEMS DESIGN
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – I

Course Code:	**P22MECE12**	**Credits:**	**04**
Teaching Hours/Week (L:T:P):	**4 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**52**	**SEE Marks:**	**50**

Course Learning Objectives: At the end of the course the students should be able to:

- Provide general approach to Embedded System (ES) design
- Understand the role of different CPU components in Embedded System design and their influence on performance.
- Provide understanding of different programming models
- Discuss the basics of operating system and different scheduling algorithms for real time applications.
- Describe program optimization, safety and security design issues in embedded designs.

UNIT – I	**11 Hours**

Embedded Computing: Introduction, Complex Systems and Microprocessors, The embedded system design process.
CPU Components: Introduction, Programming input and output, Supervisor mode, exceptions, and traps
Text 1: 1.1, 1.2,1.3, 3.1, 3.2, 3.3

Self-Study Component:	1. Design a simple model train controller using an ARM microcontroller, implementing a FIR filter to process sensor data.

UNIT – II	**10 Hours**

CPU Components: Memory system mechanisms, CPU Performance, CPU power consumption, Safety and security.
Computing Platforms: Introduction, Basic Computing Platforms, Memory Devices and Systems, Designing with computing platforms, Platform-level performance analysis, Platform-level power management.
Text 1:3.5, 3.6, 3.7, 3.8, 4.1, 4.2, 4.4, 4.5, 4.7, 4.8.

Self-Study Component:	1. Illustrate and present the concept of CPU bus and consumer electronics architecture.

UNIT – III	**11 Hours**

Embedded firmware design and development: Embedded firmware design approaches, Embedded firmware development languages, Programming in Embedded C
Text 2:Chapter 9

Self-Study Component:	1. Develop an embedded program using while loop, string operations, arrays and pointers for any real time application.

UNIT – IV	**10 Hours**

Real-Time Operating System (RTOS): Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task

Synchronization, Device Drivers.
Text 2:10.1 to 10.9

Self-Study Component:	1. Describe how different scheduling scheme handles tasks with different priorities, arrival times, and burst times and also Interpret the performance metrics used to evaluate scheduling schemes.

UNIT – V	**10 Hours**

System Design Techniques and Embedded Multiprocessors: System Design Techniques: Design Methodologies, Requirement Analysis, Specifications, System analysis and architecture design, dependability, safety and security
Embedded Microprocessors: Introduction, Why multiprocessors? Categories of multiprocessors, MPSOCs and shared memory multiprocessors,
Text1: **7.2, 7.3, 7.4, 7.5, 7.6, 10.2, 10.3, 10.4, 10.5**

Self-Study Component:	1. Analyze and present the Optical Disk as Application Example and Video Accelerator as Design example.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Apply** the basic knowledge of embedded system to **interpret** and **analyze** the various functional requirements for embedded computing designs.	L2	PO1[L2]
CO2	**Analyze** different issues involved in embedded system development using real time operating systems.	L2	PO1[L2]
CO3	**Design** and **develop** code for different embedded firmware designs.	L3,L4	PO4[L3] PO5[L4]
CO4	**Analyze** various embedded system design techniques and incorporate the same for developing specified design requirements.	L3	PO3[L3], PO5[L3]

Text Book(s):

2. Marilyn Wolf, **"Computers as Components- Principles of Embedded Computing System Design",** 4th edition, Morgan Kaufman Publications, ISBN: 978-0-12-805387-4, 2017.
3. Shibu K V, **"Introduction to Embedded Systems",** TMH Education Pvt Ltd, 2nd reprint, ISBN (13): 978-0-07-014589-4, 2010.

Reference Book(s):

5. James K Peckol, John Weily, **"Embedded Systems – A contemporary Design Tool"**, Edition, ISBN-13: 978-0471721802, ISBN-10: 9780471721802, 2008.
6. Arnold S. Berger**, "Embedded Systems Design: An Introduction to Processes, Tools, and Techniques"**, ISBN: 1578200733 CM.

Web and Video link(s):
2. https://nptel.ac.in/courses/106105159
3. https://www.youtube.com/watch?v=y9RAhEfLfJs

E-Books/Resources:

1. http://library.lol/main/256670AA7C128EF52498575367ABCB80
2. .https://archive.org/details/K.ShibuIntroductionToEmbeddedSystemsTmh2009/page/n21/mode/2up

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2	3				
#3				2	2
#4			1		2

Digital System design using Verilog
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – I

Course Code:	**P22MECE13**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 2**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: At the end of the course the students should be able to:

1. Understand the concepts of Real world circuits, Models and Design methodology
2. Design and develop the Combinational and Sequential Circuits and verify using HDL.
3. Develop the Verilog coding for many applications.
4. Analyze the synthesis of Combinational and Sequential Logic.
5. Design and synthesis the data path controllers.

UNIT – I	**8 Hours**

Introduction and Methodology: Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Models, Design Methodology.

Combinational Basics: Boolean Functions and Boolean algebra, Binary Coding, Combinational Components and Circuits.

Text 1: 1.1, 1.2, 1.4, 1.5, 2.1, 2.2, 2.3.

Self-Study Component:	2. Real-World Circuits: Integrated Circuits, Logic levels, Static Load Levels, Capacitive Load and Propagation Delay, Wire Delay, Verification of Combinational Circuits.

UNIT – II	**8 Hours**

Number Basics: Unsigned and Signed Integers, Fixed and Floating-point Numbers.

Sequential Basics: Storage elements, Counters, Sequential Datapath and Control.

Text 1: 3.1-3.4, 4.1-4.3.

Self-Study Component:	2. Clocked Synchronous Timing Methodology: Asynchronous Inputs, Verification of Sequential Circuits, Asynchronous Timing Methodologies.

UNIT – III	**8 Hours**

Memories: Concepts, Memory Types, Error Detection and Correction.

Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards.

Text 1: 5.1-5.3, 6.1-6.3.

Self-Study Component:	3. Interconnection and Signal Integrity: Differential Signaling.

UNIT – IV	**8 Hours**

Synthesis of Combinational and Sequential Logic: Introduction to Synthesis, Synthesis of Combinational Logic, Synthesis of Sequential Logic with Latches, Synthesis of Sequential Logic with Flip-Flops, Synthesis of Explicit State Machines, Registered Logic, Synthesis of Implicit State Machines, Registers, and Counters, Resets.

Text 2: 6.1-6.3, 6.5, 6.6 [excluding 6.6.4], 6.7, 6.9, 6.10.

Self-Study Component:	2. Synthesis of Three State Devices and Bus Interfaces, State Encoding.

UNIT – V	**8 Hours**

Design and Synthesis of Datapath Controllers: Partitioned Sequential Machines, Design Example: Binary Counter, Design and Synthesis of a RISC Stored-Program Machine, Design Example: UART.

Text 2: 7.1-7.4(excluding 7.4.3).

Self-Study Component:	3. UART Receiver.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	Apply the knowledge of digital circuits and Verilog HDL for real time applications.	L1,L2	PO1
CO2	Analyze the different digital circuits like memory counter, data paths, PLD's etc.	L2,L3	PO2
CO3	Develop the synthesis model of digital systems.	L4,L5	PO2
CO4	Design and develop the digital systems using EDA/CAD tools.	L4,L5	PO2,PO3

Text Book(s):

4. "**Digital Design: An Embedded Systems Approach Using VERILOG",** Peter J. Ashenden, Elesvier, ISBN 978-0-12-369527-7(2008), 9788131216637(2009), 2010.
5. "**Advanced Digital Design With the Verilog HDL"**, Michael D. Ciletti, 2nd edition, PHI, ISBN: 978–0–07–338054–4 2015.

Reference Book(s):

7. "**Verilog HDL: A Guide to Digital Design and Synthesis**" Samir Palnitkar 2nd edition Pearson, ISBN: 9788177589184 (2003) 2013.

Web and Video link(s):

4. https://nptel.ac.in/courses/106/105/106105165/#download_videos Lectured by Prof. Indranil Sengupta, IIT Kharagpur.

E-Books/Resources:

1. http://www.staroceans.org/kernel-and-driver/Digital%20Design%20-%20An%20Embedded%20Systems%20Approach%20Using%20Verilog.pdf.
2. https://www.amazon.in/Advanced-Digital-Design-Verilog-HDL/dp/933258446X.

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	**3**				
#2		**3**			
#3			**3**		
#4		**2**	**2**		

Professional Elective – I

ADVANCES IN IC FABRICATION TECHNOLOGY
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – I

Course Code:	**P22MECE141**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Provide the overview of crystal growth technique and thin film technologies.
- Explain the different lithographic process, plasma formation and etching techniques,
- Describe the deposition process of polysilicon, oxide, nitride and other materials.
- Highlight the ion implantation techniques with shallow and deep profiles.
- Discuss the metallization process and VLSI NMOS and PMOS fabrication processes.
- Provide the steps of IC memory fabrication technology and packaging schemes.

UNIT – I	**8 Hours**

Crystal Growth and Doping: Starting Growth and Doping, Growth from the Melt, Considerations for Proper Crystal Growth, Doping in the Melt, Semi-Insulating Gallium Arsenide, Properties of Melt-Grown Crystals, Solution Growth, Zone Processes, Properties of Zone-Processed Crystals.
Text1: 3.1-3.9

Self-Study Component:	3. Case study on 45 nm CMOS node Process technology

UNIT – II	**8 Hours**

Diffusion: The Nature of Diffusion, Diffusion in a Concentration Gradient, The Diffusion Equation, Impurity Behavior: Silicon, Impurity Behavior: Gallium Arsenide, Diffusion Systems, Diffusion Systems for Silicon, Special Problems in Silicon Diffusion, Diffusion Systems for Gallium Arsenide, Evaluation Techniques for Diffused Layers.
Text 1: 4.1-4.10

Self-Study Component:	3. Determine a criterion for differentiating a peritectic compound from a congruent transformation of Arsenic-Silicon system.

UNIT – III	**8 Hours**

Epitaxy: General Considerations, Molecular Beam Epitaxy, Vapor-Phase Epitaxy, VPE Processes for Silicon, VPE Processes for Gallium Arsenide, Liquid-Phase Epitaxy, LPE Systems, Heteroepitaxy, Evaluation of Epitaxial Layers.
Text 1: 5.1-5.9

Self-Study Component:	4. List the types of devices that are prepared using Epitaxy techniques.

UNIT – IV	**8 Hours**

Ion Implantation: Penetration Range, Implantation Damage, Annealing, Ion Implantation Systems, Process Considerations, High-Energy Implants, High-Current Implants.
Etching and Cleaning: Wet Chemical Etching, Dry Physical Etching, Dry Chemical

Etching, Reactive Ion Etching.

Text 1: 6.1-6.7, 9.1-9.4

Self-Study Component:	3. Make a list of the films used for interconnections in the process of IC fabrication.

UNIT – V	**8 Hours**

Lithographic Processes: Photoreactive Materials, Pattern Generation and Mask-Making, Pattern Transfer.
Device and Circuit Fabrication: Isolation, Self-Alignment, Local Oxidation, Planarization, Metallization, Gettering
Text1: 10.1-10.3, 11.1-11.6

Self-Study Component:	4. Detail study on Fully depleted Silicon on Insulator (FDSOI) devices and their applications, advanced techniques and problem areas.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	***Apply*** the basic theory of Growth and Doping. Learn the basic theory of Crystal growth and Properties of Zone-Processed Crystals.	L3	PO1, PO5
CO2	***Analysis*** of Diffusion in silicon and Gallium Arsenide and Evaluation Techniques for Diffused Layers, Ion Implantation and understand the concept of Etching and Cleaning.	L3	PO2
CO3	***Knowledge*** of Epitaxy and Evaluation of Epitaxial Layers.	L4	PO1
CO4	***Understand*** the Concepts of Lithographic Processes, Device and Circuit Fabrication.	L2	PO2, PO5

Text Book(s):

"VLSI Fabrication Principles: Silicon and Gallium Arsenide", Gandhi, S. K., John Wiley and Sons, 2nd edition,ISBN: 978-0-471-58005-8, 2008.

Reference Book(s):

1. **"Silicon VLSI Technology: Fundamentals, Practice and Modeling",** Plummer J.D., Deal, M.D. and Griffin, P.B., Pearson Education, 3rd edition, Prentice-Hall, ISBN 978-81-317-2604-4, 2000.
2. **"VLSI Technology",**S.M.Sze , 2nd edition, McGraw-Hill, **ISBN13:** 9780070627352 **ISBN10:** 0070627355,2003.
3. **"ULSI Technology",** C. Y. Chang & S. M. Sze (Editors), McGraw Hill, ISBN-10: 0070630623, ISBN-13: 978-0070630628, 1996.

Web and Video link(s):
https://nptel.ac.in/courses/117/106/117106093/#watch Lectured by Prof.NanditaDasgupta, IIT Madras.

E-Books/Resources:
1. Groover M.P, "Processing of Integrated Circuits" in Fundamentals of

Modern Manufacturing, 4th Edition, New Jersey, John Wiley & Sons, 2010, ch.34 pp 800-826.
2. Madehow.com,'IntegratedCircuit [2017].[Online]. http://www.madehow.com/Volume-2/Integrated-Circuit.html.
3. Mepits.com, 'How to manufacture an IC' [2015].[Online]. https://www.mepits.com/tutorial/384/VLSI/Steps-for-IC- manufacturing.
4. Berkeley.edu, 'The IC Manufacturing Process' [2000].[Online]. http://bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f01/Notes/chapter2.pdf.
5. Ti.com, 'Semiconductor Manufacturing: How a Chip is Made' [2017]. [Online]. http://www.ti.com/corp/docs/manufacturing/howchipmade.shtml.
6. Available: http://www.semiconductormuseum.com/Transistors/LectureHall/Camenzind/Camenzind_Index.htm
7. Quora.com, 'What is the most common example of an analog IC?' [2016]. [Online].Available:https://www.quora.com/What-is-the-most-common-example-of-an-analog-integrated-circuit.
8. Google Images, 'Image of Signetics 555 IC' [2005]. [Online].Available: https://goo.gl/eyA3G7
M.eet.com,'Microprocessor Image' [2014]. [Online].Available: http://m.eet.com/images/eetimes/2014/03/1321611/sv-0005-01.jpg.

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	2				1
#2		3			
#3	2				1
#4		2			1

PHYSICAL DESIGN
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – I

Course Code:	**P22MECE142**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Understand VLSI backend process i.e. physical design flow with significance of steps involved.
- Familiarize with the mathematical aspects of physical design and related algorithms.
- Apply the algorithms at different abstract levels of the flow for analysing the design.
- Identifying, Selecting and adopting the Floor plans, routing schemes and clock tree topologies and placement strategies.

UNIT – I	**8 Hours**

Introduction: Electronic Design Automation, VLSI Design Flow, VLSI Design Styles, Layout Layers and Design Rules, Physical Design Optimizations, Algorithms and Complexity, Graph Theory Terminology, Common EDA Technology.
Netlist and System Partitioning: Introduction, Terminology, Optimization Goals, Partitioning Algorithms: Kernighan-Lin (KL) Algorithm.
Text 1: 1.1-1.8 and2.1-2.4.1.

Self-Study Component:	4. Study the Tool Command Language (TCL). 5. Identify, list and compare proprietary/open source tools for Net list and System Partition.

UNIT – II	**8 Hours**

Chip Planning: Introduction, Optimization goals in Floor planning, Terminology, Floor plan representations.
Floor Planning Algorithms: Floor plan sizing, cluster growth, simulated annealing, Pin assignment.
Power and Ground Routing: Design of Power-Ground Distribution Network, Planar Routing, Mesh Routing.
Text 1:3.1-3.7.

Self-Study Component:	4. Analyze the synthesis report files for Area, Power and Timing. 5. Develop a code for the given Floor planning algorithm.

UNIT – III	**8 Hours**

Global Placement and Routing: Introduction, Optimization Objectives, Global placement algorithms: Min-cut placement, Analytic placement, Simulated annealing, Modern placement algorithms.
Global Routing: Introduction, Terminology and Definitions, Optimization Goals, Representations of Routing Regions, The Global Routing Flow, Single-Net Routing**:** Rectilinear routing, Finding Shortest Paths with Dijkstra's Algorithm.
Text 1: 4.1-4.3 and 5.1-5.6.

Self-Study Component:	5. Develop a code for given Placement and Routing algorithms.

UNIT – IV	8 Hours
Detailed Routing: Terminology, Horizontal and Vertical Constraint Graphs, Channel Routing Algorithms, Switchbox Routing, Over-the-Cell Routing Algorithms. **Specialized Routing:** Introduction to Area Routing, Net Ordering in Area Routing, Non-Manhattan Routing, Basic Concepts in Clock Networks **Text 1: 6.1-6.4 and 7.1-7.4.**	
Self-Study Component:	1. Place and route steps for any design using cadence innovous/encounter
UNIT – V	**8 Hours**
Timing Closure: Introduction, Timing Analysis and Performance Constraints, Timing-Driven Placement, Timing-Driven Routing, Physical Synthesis, Performance-Driven Design Flow. **Text1: 8.1-8.6.**	
Self-Study Component:	5. Clock tree synthesis steps for any design using cadence innovous/encounter. 6. Investigate the given circuits for timing constraints.

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	***Apply*** the knowledge of graph theory in VLSI Physical Design.	L2	PO1 [L2]
CO2	***Analyze*** the VLSI Design through partitioning, place and route with clock tree.	L3	PO3[L3]
CO3	***Evaluate*** the impact of different Physical Design algorithms at various abstract levels.	L4	PO1,PO4 [L4]
CO4	***Discuss*** the relation and impact of design constraints on Physical Design.	L5	PO3, PO5 [L5]

Text Book(s):

1. **"VLSI Physical Design: From Graph Partitioning to Timing Closure"**, Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, 1st edition, Springer, 2011 ISBN 978-90-481-9590-9 e-ISBN 978-90-481-9591-6

Reference Book(s):

1. **"Algorithms for VLSI Design Automation"**, Sabih H. Gerez, ISBN: 9780471984894, 0471984892, 2000.
2. **"Handbook of Algorithms for Physical design Automation",** Charles J. alpert, Dinesh p. Mehta, Sachin S. Sapatnekar. ISBN: 9780849372421, 0849372429
3. **Algorithms for VLSI Physical Design Automation"**, N. A. Shervani, 1999. 3rd edition ISBN 0-7923-8393-1

Web and Video link(s):

1. https://www.youtube.com/playlist?list=PLCmoXVuSEVHlEJi3SwdyJ4EICffuyqpjk
2. https://www.youtube.com/playlist?list=PLDYvivDnqWMMNIOh511ep2sr6nmlhMIn

Y

E-Books/Resources:

1. https://www.ifte.de/books/eda/index.html
2. https://anysilicon.com/introduction-to-physical-design/

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2			3		
#3	3			3	
#4			3		2

SYSTEM ON CHIP
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – I

Course Code:	**P22MECE143**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Compare the performance, advantages, and disadvantages of system on board, system on chip, and system in package.
- Able to learn about how the system forms with the lot of component and has majority about system level interconnections.
- Equipped to introduce hardware and software programmability versus performance.
- Competent in understanding the entire memory organization, scratch pads, cache memories, and the objectives in cache data, including how to handle the write policies.
- Describe the AMBA, NOC, Customization and Configurability.

UNIT – I	**8 Hours**

Introduction to the systems approach: System Architecture: An Overview, Components of the System: Processors, Memories, and Interconnects Hardware and Software: Programmability, Versus Performance, Processor Architectures-Processor: A functional view, Processor: An architectural view, Memory and Addressing, SOC Memory Examples, Addressing: The architecture of Memory, Memory for SOC Operating System, System - Level Interconnection, Bus - Based Approach, Network - on - Chip Approach, An Approach for SOC Design, Requirements and Specifications, Design Iteration, System Architecture and Complexity, Product Economics and Implications for SOC Dealing with Design Complexity.

Text 1: 1.1-1.10

Self-Study Component:	6. Identify the applications of SOC in today electronics industry. 7. Prepare the report on the tools available for the SOC Design.

UNIT – II	**8 Hours**

Chip Basics: Time, Area, Power, Reliability, and Configurability-Introduction, Design Trade – Offs, Cycle Time, The Pipelined Processor, Defining A Cycle, Optimum Pipeline, Performance, Die Area and Cost, Processor Area, Ideal and Practical Scaling, Power, Area – Time – Power Trade - Offs in Processor Design.

Processors: Processor Selection for SOC: Overview, Examples: Processor Core Selection, Basic Concepts in Processor Architecture, Instruction Set, Some Instruction Set Conventions, Branches, Interrupts and Exceptions, Basic Concepts in Processor Microarchitecture, Basic Elements in Instruction Handling-The Instruction Decoder and Interlocks, Buffers: Minimizing Pipeline Delays, More Robust Processors: Vector, Very Long Instruction Word (VLIW)and Superscalar, Vector Processors and Vector Instruction Extensions, Vector Functional Units, VLIW Processors.

Text 1: 2.1-2.6, 3.2,3.2.1,3.2.3,3.3-3.5,3.5.1,3.6,3.6.1,3.8,3.9

Self-Study Component:	6. Discuss the Area Estimate of Reconfigurable Devices. 7. Prepare the report on the recent Processor are used in Computers,

	laptop, mobiles.
UNIT – III	**8 Hours**
Memory Design: System- on- Chip and Board - Based Systems- Introduction, SOC External Memory: Flash, SOC Internal Memory: Placement, The Size of Memory, Scratchpads and Cache Memory, Basic Notions, Cache Organization, Cache Data, Write Policies, Strategies for Line Replacement at Miss Time, Fetching A Line, Line Replacement, Cache Environment: Effects of System, Transactions and Multiprogramming, Other Types of Cache, Split I - and D - Caches and the Effect of Code Density, Multilevel Caches, Limits on Cache Array Size, Evaluating Multilevel Caches, Logical Inclusion, Virtual - to - Real Translation, SOC (On - Die) Memory Systems, Board - Based (Off - Die) Memory Systems, Simple Dram and The Memory Array, SDRAM and DDR SDRAM, Memory Buffers, Models of Simple Processor – Memory Interaction, Models of Multiple Simple Processors and Memory. **Text 1:4.1-4.16,4.16.1**	
Self-Study Component:	6. Compare the difference between SDRAM and DDR SDRAM. 7. Prepare the report on in today electronics industry.
UNIT – IV	**8 Hours**
Interconnect: Introduction, Overview: Interconnect Architectures, Bus: Basic Architecture, Arbitration and Protocols, Bus Bridge, Physical Bus Structure, Bus Varieties, SOC Standard Buses, AMBA, Core Connect, Bus Interface Units: Bus Sockets and Bus Wrappers, Analytic Bus Models, Contention and Shared Bus, Simple Bus Model: Without Resubmission, Bus Model with Request Resubmission, Using The Bus Model: Computing the Offered Occupancy, Effect of Bus Transactions and Contention Time, Beyond the Bus: NOC with Switch Interconnects, SOC interconnect Switches, Static Networks, Dynamic Networks, Some NOC Switch Examples, Asynchronous Crossbar Interconnect for Synchronous SOC, (Dynamic Network), Blocking Versus Non blocking, Layered Architecture and Network Interface Unit, NOC Layered Architecture, Bus Versus NOC, Evaluating Interconnect Networks, Static Versus Dynamic Networks. **Text 1:5.1-5.8,5.8.1,5.8.3,5.9,5.9.1.**	
Self-Study Component:	4. Identify the usage of AMBA in real time. 5. Discuss the tools are available for the NOC design.
UNIT – V	**8 Hours**
Customization and Configurability: Introduction, Estimating Effectiveness of Customization, Soc Customization: An Overview, Customizing Instruction Processors, Processor Customization Approaches, Architecture Description, Identifying Custom Instructions Automatically, Reconfigurable Technologies, Reconfigurable Functional Units (FUS), Reconfigurable Interconnects, Software Configurable Processors , Mapping Designs onto Reconfigurable Devices, Instance - Specific Design, Reconfiguration, Reconfiguration Overhead Analysis, Trade - Off Analysis: Reconfigurable Parallelism. **Application Studies:** Application Study: AES - algorithm and requirements, - 3D graphics processors, image compression, video compression, MP3 audio decoding. **Text 1:6.1,6.2,6.3,6.4,6.5,6.6,6.7,6.9,7.3,7.3.1,7.4,7.5,7.6,7.7.1.**	

Self-Study Component:	7. Compare the difference between AES and DES. 8. Identify the different algorithms used in video compression.

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	**Demonstrate** comprehensive knowledge of system architecture, including an overview of components such as processors, memories, and interconnects.	L2	PO1 [L2]
CO2	**Illustrate** a functional and architectural view of processors, addressing memory and addressing schemes in SoC designs.	L2	PO1 [L2]
CO3	**Apply** knowledge of design trade-offs concerning time, area, power, reliability, and configurability in chip design.	L3	PO1 [L2] PO2 [L3]
CO4	**Analyze** the performance of interconnect architectures, including bus and NoC, and their impact on system efficiency.	L3	PO3 [L3]
CO5	**Interpret** various types of memory used in SoC, both external and internal, including their placement, size, and management strategies.	L5	PO3 [L4] PO4 [L5]

Text Book(s):

1. **"Computer System Design System-On-Chip"** Michael J. Flynn, Wayne Luk, A John Wiley & Sons, Inc., Publication, ISBN: 9781118009925, 2011.

Reference Book(s):

1. **"Reuse Methodology Manual for System-On-A-Chip",** Michael Keating, Designs, Pierre Bricaud,2nd edition, Kluwer Academic Publishers, ISBN: 9781461550372, 2001.
2. **"SoC Verification-Methodology and Techniques",** Prakash Rashinkar, Peter Paterson and Leena Singh, Kluwer Academic Publishers, ISBN – 8580000264227, 2001.
3. **"On-Chip Communication Architectures: System on Chip Interconnect",** Sudeep Pasricha and B Nikil B Dutt, Morgan Kaufmann Publishers, 978-0-12-373892-9, 2008.

E-Books/Resources:
https://books.google.co.in/books?hl=en&lr=&id=QXtyqHryAL4C&oi=fnd&pg=PR13&dq=1.%09%E2%80%9CComputer+System+Design+System-On-Chip%E2%80%9D+Michael+J.+Flynn,+Wayne+Luk,+A+John+Wiley+%26+Sons,+Inc.,+Publication,+ISBN:+9781118009925,+2011.&ots=nBpd_aFf2U&sig=qvYkpLr5_e0uxh4r7YPMBEWZOl0&redir_esc=y#v=onepage&q=1.%09%E2%80%9CComputer%20System%20Design%20System-On-Chip%E2%80%9D%20Michael%20J.%20Flynn%2C%20Wayne%20Luk%2C%20A%20John%20Wiley%20%26%20Sons%2C%20Inc.%2C%20Publication%2C%20ISBN%3A%209781118009925%2C%202011.&f=false

Course Articulation Matrix (CAM)					
CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**
#1	**3**				
#2	**2**				
#3		**2**			
#4			**3**		
#5				**2**	

INTERNET oF THINGS

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – I

Course Code:	**P22MECE144**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Describe the basics, definition and vision of Internet of Things (IOT).
- Analyse IOT in terms of a suggested IOT conceptual framework.
- Illustrate the usage of messaging protocols between connected devices and the web.
- Apply the data-acquiring and data-storage functions for IOT/M2M devices data and messages and Classify ways of organizing data.
- Describe cloud computing service models in a software architectural concept, everything as a service (XAAS).
- Learn the usage of cloud platforms for IOT applications and services with examples of Xively(Pachube/COSM) and Nimbits.
- Describe the uses of actuators, data communication using serial bus protocols.

UNIT – I	**10 Hours**

Internet of Things: an Overview: Internet of things, IOT Conceptual Framework, IOT Architectural View, Technology Behind IOT, Sources of IOT, M2M Communication.
Design Principles for Connected Devices: Introduction, IOT/M2M Systems Layers and Design Standardization, Communication Technologies, Data Enrichment, Data Consolidation and Device Management at Gateway, Ease of Designing and Affordability.
Text 1: 1.1-1.6, 2.1-2.5.

Self-Study Component:	1. Illustrate the importance of IOT in today's reality applications. 2. Kavre, M., Gadekar, A., & Gadhade, Y. (2019, December). Internet of Things (IoT): a survey. In *2019 IEEE pune section international conference (PuneCon)* (pp. 1-6). IEEE.

UNIT – II	**10 Hours**

Design Principles for Web Connectivity: Introduction, Web Communication Protocols for Connected Devices, Message Communication Protocols for Connected Devices, Web connectivity for Connected- Devices Network using Gateway, SOAP, REST, HTTP RESTful and WebSockets.
Internet Connectivity Principles: Internet –Based communication, IP Addressing in IOT.
Text 1: 3.1-3.4, 4.3, 4.4.

Self-Study Component:	8. Understand the functionalities of HTTP, HTTPS, FTP, Telnet, CoAP and LWM2M. 9. Analyze and interpret the various Internet Communication protocols for practical applications.

UNIT – III	**11 Hours**

Data Acquiring, Organizing, Processing: Introduction, Data Acquiring and Storage, Organizing the Data, Transaction, Business Processes, Integration and Enterprise Systems.
Data Collection, Storage and Computing Using a Cloud Platform: Introduction, Cloud Computing Paradigm for Data Collection, Storage and Computing, Everything as a Service

and Cloud Service Models, IOT Cloud-Based Services Using the Xively, Nimbits and Other Platforms. **Text 1: 5.1, 5.2, 5.3, 5.4, 6.1-6.4.**	
Self-Study Component:	1. Analysis of the sensor devices currently available with a brief presentation on the same. 2. Analyzing the working of Radio Frequency Identification Technology.
UNIT – IV	**10 Hours**
Sensors, Actuators, RFIDs: Introduction, Sensor Technology, Participatory Sensing, Industrial IOT and Automotive IOT. Actuator, Sensor Data Communication Protocols. **Prototyping and Designing the Software for IOT Applications:** Introduction, Prototyping Embedded Device Software, Devices, Programming Embedded Device Arduino Platform using IDE, Reading from the Sensors and Devices. **Text 1: 7.1, 7.2, 7.3, 7.4, 7.5, 9.1, 9.2,9.2.1, 9.2.2**	
Self-Study Component:	1. Programming Embedded Galileo, Raspberry Pi, BeagleBone and mBed Device Platforms. 2. Programming Embedded Device Platforms for Internet Connectivity Using the Ethernet and WiFi Libraries.
UNIT – V	**11 Hours**
Internet of Things Privacy, Security and Vulnerabilities Solutions: Introduction, Vulnerabilities, Security Requirements and Threat Analysis, Use cases and Misuse Cases, IOT Security Tomography and Layered Attacker Model, Identity Management and Establishment, Access Control and Secure Message Communication, Security Model, Profiles and Protocols for IOT. **Text 1: 10.1-10.6**	
Self-Study Component:	1. Understand and present Design Complexity and Designing Using Cloud Paas. 2. Develop IOT Application for Smart Homes, Smart Environment Monitoring and Smart Agriculture.

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	**Apply** the knowledge of digital electronics, Microcontroller and communication principles to describe fundamental elements of IoT.	L3	PO1[L3]
CO2	**Analyze** design principles of connected devices, web connectivity, internet connectivity and software for current IoT Applications along with security and privacy vulnerabilities.	L2,L3	PO4 [L2, L3]
CO3	**Illustrate and interpret** various sensors and actuators used to implement IoT applications along with data analysis for cloud platform.	L3,L4	PO1[L3] & PO4 [L3]
CO4	**Design** and **Develop** IoT model for given specifications using embedded software.	L5	PO5 [L5]

Text Book(s):

2. Raj kamal, **"Internet of Things: Architecture and Design Principles"**, McGraw Hill, 1 st edition, 5 the Reprint ,2019, ISBN-13: 978-9352605224.

Reference Book(s):

1. Arshdeep Bahga, Vijay Madisetti, **"Internet of Things: A Hands on Approach"**, Orient Blackswan Private Limited - New Delhi; 1st edition ,2015, ISBN-13: 978-8173719547.
2. HakimaChaouchi, **"The Internet of Things Connecting Objects to the Web"**, Willy Publications, 2017, ISBN-13: 978-8126566839

Web and Video link(s):

5. https://nptel.ac.in/courses/106/105/106105166
6. https://www.digimat.in/nptel/courses/video/106105166/L01.html
7. https://www.youtube.com/watch?v=xsZ9YhVy-7g

E-Books/Resources:

1. https://dokumen.pub/internet-of-things-9352605225-9789352605224.html.

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2				3	
#3	2			2	
#4					1

Professional Elective – II

ASIC DESIGN

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – I

Course Code:	**P22MECE151**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Provide the knowledge of ASIC Design Flow.
- Cover Fundamentals of Full custom, Semi custom and standard cell based design.
- Explain the low-level design entry.
- Application of Low Level Design Languages.
- Describe the various concepts of floor planning and placement and routing and partitioning methods.

UNIT – I	**8 Hours**

Introduction: Full Custom with ASIC, Semi custom ASICS, Standard Cell based ASIC, Gate array based ASIC, Channeled gate array, Channel less gate array, structured get array, Programmable logic device, FPGA, Design flow, ASIC cell libraries.

Text 1: 1.1(1.1.1 to 1.1.8), 1.2,1.5.

Self-Study Component:	8. Case Study, Carry out the survey on ASIC ICs which are used in industries.

UNIT – II	**8 Hours**

Data Path Logic Cells: Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers, ASIC Library Design: Logical effort, predicting delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum number of stages, library cell design.

Text 1: 2.6,2.6.1,2.6.2,2.6.4,2.6.5, 2.7,2.8, 3.3, 3.4.

Self-Study Component:	10. Other Data path Operators, Library Architecture, Gate array Design.

UNIT – III	**8 Hours**

Low-Level Design Entry: Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist Screener.

Text 1: 9.1, 9.1.1- 9.1.13.

Self-Study Component:	8. Schematic –Entry tools and Back annotation.

UNIT – IV	**8 Hours**

Low Level Design Languages: ABEL, CUPL, PALASM, PLA Tools, EDIF, an introduction to CFI designs representation.

Text 1: 9.2,9.2.1,9.2.2,9.2.3,9.3, 9.4,9.4.1,9.4.2,9.5.

Self-Study Component:	1. Introduction to Synthesis and Simulation.

UNIT – V	**8 Hours**

ASIC Construction: Physical Design ,System Partitioning, Estimating ASIC size. Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative

placement improvement, Time driven placement methods. Physical Design flow
Text1: 15.1, 15.3, 15.4, 16.1.3, 16.1.5, 16.1.6, 16.2.4, 16.2.6, 16.2.8,16.3

Self-Study Component:	1. Partitioning methods, Global Routing, Detail Routing, Special Routing.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Understand** the various types of ASICs including full custom, semi-custom, standard cell-based, and gate array-based ASICs, and differentiate their applications and design methodologies.	L1	PO1[L1],PO2[L2]
CO2	**Apply** logical effort analysis to evaluate and optimize ASIC library cells for efficient circuit design, predicting delay, area, and logical efficiency.	L2	PO2[L2]
CO3	**Analyze** the schematic entry tools to design hierarchical ASIC circuits, ensuring accurate representation of circuit components, connectivity, and hierarchical organization.	L2, L3	PO2[L2] &PO3[L3]
CO4	**Implement** ASIC designs using low-level design languages such as ABEL and CUPL, and interpret EDIF formats for seamless integration into ASIC design flows.	L4	PO4[L4] &PO5[L4]
CO5	**Execute** the physical design flow of ASICs, including system partitioning, floor planning, and placement algorithms to achieve optimal chip size, power distribution, and performance targets.	L4	PO4[L4] &PO5[L4]

Text Book(s):

1. "**Application - Specific Integrated Circuits**", M.J.S .Smith, Pearson Education 1st Edition, 2003.ISBN-13: 978-8177584080.

Reference Book(s):

1. "Design of Analog-Digital VLSI Circuits for Telecommunication and Signal Processing" Jose E.France, Yannis T sividis, 2nd Edition**,** Prentice Hall, 1994. ISBN-13: 978-0132036399.

2. **"Analog VLSI Design – NMOS and CMOS",** MalcolmR.Haskard; Lan. C. May, Prentice Hall, 1st Edition, 1998. ISBN-13: 978-0130326409.

Web and Video link(s):

1. https://www.youtube.com/watch?v=oZSv68esbgI
2. https://www.youtube.com/watch?v=zpOioOiKYp4
3. https://www.youtube.com/watch?v=B0ctVRjOK1o

E-Books/Resources:

1. https://asicdigitaldesign.wordpress.com/recommended-reading/
2. https://pg024ec.wordpress.com/wp-content/uploads/2013/09/01_asic-book-by-michael-smith.pdf

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2		2		2	
#3	3	3	2		
#4				2	2
#5				2	2

MEMS AND SENSORS

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – I

Course Code:	**P22MECE152**	**Credits:**	03
Teaching Hours/Week (L:T:P):	3 : 0 : 0	**CIE Marks:**	50
Total Number of Teaching Hours:	40	**SEE Marks:**	50

Course Learning Objectives (CLOs)

This course will enable the students to:

1. Discuss the overview of microsystems, their fabrication and application areas.
2. Understand the working principles of several MEMS devices.
3. Develop mathematical and analytical models of MEMS devices.
4. Understand the methods to fabricate MEMS devices.
5. Provide the knowledge of various application areas where MEMS devices can be used.

UNIT – I	**8 Hours**

Introduction: Why Miniaturization, Microsystems Versus MEMS, Why Microfabrication, Smart Materials, Structures and Systems, Integrated Microsystems, Applications of Smart Materials and Microsystems,

Micro Sensors, Actuators, Systems and Smart Materials: **An Overview:** Silicon Capacitive Accelerometer, Piezoresistive Pressure Sensor, Conductometric Gas Sensor, Fiber-Optic Sensors, Electrostatic Comb-Drive, Magnetic Microrelay, Microsystems at Radio Frequencies, Portable Blood Analyzer, Piezoelectric Inkjet Print Head, Micromirror Array for Video Projection, Micro-PCR Systems.

Text1:1- 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 2- 2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8, 2.9, 2.10, 2.11.

Self-Learning Component:	Summary of the microfabrication, Smart Materials Systems and Micro sensors.

UNIT – II	**8 Hours**

Micromachining Technologies: Silicon as a Material for Micromachining, Thin-film Deposition, Lithography, Doping the Silicon Wafer: Diffusion and Ion Implantation of Dopants, Etching, Dry Etching, Silicon Micromachining, Specialized Materials for Microsystems.

Text 1: 3 – 3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7.

Self-Learning Component:	Case Study of Advanced Microfabrication Processes and Specialized for Microsystems.

UNIT – III	**8 Hours**

Mechanics of Slender Solids in Microsystems: The Simplest Deformable Element: A Bar, Transversely Deformable Element: A Beam, Energy Methods for Elastic Bodies, Examples and Problems, Heterogeneous Layered Beams, Bimorph Effect, Residual Stresses and Stress Gradients, Poisson Effect and the Anticlastic Curvature of Beams, Torsion of Beams and Shear Stresses, Dealing with Large Displacements, In-Plane Stresses.

The Finite Element Method: Need for Numerical Methods for Solution of Equations, Variational Principles, Weak Form of the Governing Differential Equation, Finite Element Method, Numerical Examples, Finite Element Formulation for Time-Dependent Problems, Finite Element Model for Structures with Piezoelectric Sensors and Actuator.

Text 1:4 – 4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9, 4.10, 4.11, 5 – 5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7.

Self-Learning Component:	Study on Integrated Microsystems and Dynamics and Analysis of a Piezoelectric Bimorph Cantilever Beam.

UNIT – IV	**8 Hours**

Modeling of Coupled Electromechanical Systems: Electrostatics, Coupled Electromechanics: Statics, Coupled Electromechanics: Stability and Pull-In Phenomenon, Coupled Electromechanics: Dynamics, Squeezed Film Effects in Electromechanics, Electro-Thermal-Mechanics, Coupled Electromagnet-Elastic Problem.
Text 1:6 – 6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 6.7.

Self-Learning Component:	Case Study on Smart Structure in Vibration Control and Scaling in Magnetic Domain

UNIT – V	**8 Hours**

Electronics Circuits and Control for Micro and Smart Systems: Semiconductor Devices, Electronics Amplifiers, Signal Conditioning Circuits, Practical Signal conditioning Circuits for Microsystems, Introduction to Control Theory, Implementation of Controllers.
Integration of Micro and Smart Systems: Integration of Microsystems and Microelectronics, Microsystems Packaging, Mechanisms.
Text 1: 7 – 7.1, 7.2, 7.3, 7.4, 7.5, 7.6, 8 - 8.1& 8.2.

Self-Learning Component:	Case Study on Smart system and Scaling in Biochemical Phenomena.

Course Outcomes: On completion of this course, students are able to:

CO #	Course Outcome	Program Outcome Addressed (PO #) with BTL
CO1	**Apply**the technologies related to Micro Electro Mechanical Systems.	PO1 [L3]
CO2	Analyse the MEMS devices and develop suitable mathematical models.	PO2 [L4]
CO3	Design and Develop the fabrication processes involved with MEMS devices.	PO3,PO4 [L4,L5]
CO4	Design the MEMS devices for various application areas.	PO3 [L4]

Text Book(s):

1. **"Micro and Smart Systems"** byDr.A.K.Aatre, Ananth Suresh, K.J.Vinoy, S. Gopalakrishna, K.N.Bhat., John Wiley Publications, 2002, ISBN: 1118213904, 97811182139022.

Reference Book(s):

1. **"MEMS & Microsystems: Design and Manufacture"**, Tai-Ran Tsu, Tata Mc-Graw-Hill.2002.8th reprint, ISBN-13:978-0-07-048709-3. ISBN-10:0-07-048709-X
2. **"RF MEMS Theory, Design and Technology GABRIEL M. REBEIZ"**, 2003 A John Wiley & Sons Publication. ISBN: 978-0-471-20169-4 4.
3. **"Microsystems Design"**, S. D. Senturia, Kluwer Academic Publishers, Boston, USA, 2001, ISBN 0-79237246-8.

Web and Video link(s):

1. https://nptel.ac.in/courses/117/105/117105082/#watchLectured by Prof.SantiramKal, IIT Kharagpur.

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2		3			
#3			3	3	
#4			2		

Applications of Machine Learning In VLSI

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – I

Course Code:	**P22MECE153**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3** : 0 : 0	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Understand the fundamentals of Neural Network and Deep Learning
- Introduce to the concepts of NVDIA GPU, Tensor Processing Unit.
- Learn streaming graph Theory.
- Learn In-Memory Computation.
- Familiarize Near-Memory Architecture.
- Introduce Machine learning concepts in physical verification and design.
- Understand statistical analysis of SRAM using Machine learning.

UNIT – I	**8 Hours**

Introduction: Development History, Development History, Neural Network Models, Neural Network Classification , Neural Network Framework, Neural Network Comparison.
Deep Learning: Neural Network Layer, Deep Learning Challenges.
Parallel Architecture: Intel Central Processing Unit (CPU), NVIDIA Graphics Processing Unit (GPU).
Text 1: • Chapter 1, Chapter 2, 3.1, 3.2.

Self-study component:	1. Formulate MATLAB functions for neural network.

UNIT – II	**8 Hours**

Parallel Architecture: NVIDIA Deep Learning Accelerator (NVDLA), Google Tensor Processing Unit (TPU). Microsoft Catapult Fabric Accelerator
Streaming Graph Theory: Blaize Graph Streaming Processor, Graphcore Intelligence Processing Unit
Convolution Optimization: Deep Convolutional Neural Network Accelerator
In-Memory Computation: Neurocube Architecture,
Text 1: • 3.3,3.4,3.5,4.1,4.2,5.1, 6.1

Self-study component:	1. Interpret Architecture of Qualcomm Snapdragon 888

UNIT – III	**8 Hours**

In-Memory Computation: Neurocube architecture, Tetris Accelerator, Neuro Stream Accelerator
Near-Memory Architecture: DaDianNao Supercomputer, Cnvlutin Accelerator.
Network Sparsity: Energy Efficient Inference Engine (EIE), Cambricon-X Accelerator
3D Neural Processing: 3D Integrated Circuit Architecture, Power Distribution Network, 3D Network Bridge, Power-Saving Techniques

Text 1: • 6.1, 6.2, 6.3 ,7.1,7.2,8.1,8.2,9.1,9.2,9.3,9.4

Self-study component:	1. Illustrate supercomputer architectures

UNIT – IV	**8 Hours**

Machine Learning in Physical Verification, Mask Synthesis, and Physical Design: Introduction, Machine Learning in Physical Verification, Machine Learning in Physical Design
Machine Learning-Based Aging Analysis : Introduction, Negative Bias Temperature Instability, Related Prior Work, Proposed Technique, Offline Correlation Analysis and Prediction Model, Runtime Stress Monitoring, Results, Conclusions

Text 2: • Chapter 4 and Chapter 9	
Self-study component:	1. Summarize the Machine Learning Applications in VLSI routing.

UNIT – V	**8 Hours**

Extreme Statistics in Memories: Cell Failure Probability: An Extreme Statistic, Extremes: Tails and maxima

Fast Statistical Analysis Using Machine Learning: Introduction: Logistic Regression-Based Importance Sampling Methodology for Statistical Analysis of Memory Design, Application to State-of-the-Art FinFET SRAM Design

Text 2: • Chapter 10 and 11.1,11.5

Self-study component:	1. Illustrate the Machine Learning regression techniques and sampling algorithms.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	Understand the concepts of Neural Network and Deep learning	L2	PO1 [L2]
CO2	Understand the concepts of Parallel Architecture and Streaming Graph Theory	L2	PO2[L2]
CO3	Analyze In-memory computation and Near-memory architecture.	L3	PO4[L3]
CO4	Apply the knowledge of Machine Leaning in Physical verification, physical design and aging analysis.	L4	PO4[L4]
CO5	Analyze the statistical analysis in Memory Design.	L3	PO3[L3]

Text Book(s):

1. Albert Chun Chen Liu, Oscar Ming Kin Law , **"Artificial Intelligence Hardware Design: Challenges and Solutions"**, IEEE Press, Wiley, ISBN: 9781119810452
2. Ibrahim(Abe)M.Elfadel, DuaneS.Boning, Xin_Li, **"Machine Learning in VLSI Computer- Aided Design",** Springer, ISBN 978-3-030-04665-1

Reference Book(s):

1. Stuart J. Russell and Peter Norvig , **"Artificial Intelligence :A Modern Approach"**, *Prentice Hall,4th Edition,1995.*
2. Sandeep Saini, Kusum Lata, and G.R. Sinha, **"VLSI And Hardware Implementations Using Modern Machine Learning Methods"**, CRC Press 2022, ISBN: 978-1-032-06171-9 (hbk) ISBN: 978-1-032-06172-6 (pbk) ISBN: 978-1-003-20103-8 (ebk) DOI: 10.1201/9781003201038

Web and Video link(s):

1. https://archive.nptel.ac.in/courses/106/105/106105152/
2. http://digimat.in/nptel/courses/video/106106139/L01.html

E-Books/Resources:

https://www.oreilly.com/library/view/machine-learning-techniques/9781119910398/
https://www.google.co.in/books/edition/Machine_Learning_and_Artificial_Intellig/ybyxDwAAQBAJ?hl=en&gbpv=1&dq=books+on+ai+and+ml&printsec=frontcover

Course Articulation Matrix (CAM)					
CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**
#1	**2**				
#2		**2**			
#3				**2**	
#4				**3**	
#5			**3**		

HARDWARE-SOFTWARE CO-DESIGN

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – I

Course Code:	**P22MECE154**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Understand the basics of co-design models and their significance.
- Discuss the concepts of partitioning and abstraction involved in hardware and software for co-design.
- Understand the requirements of coordinating in analyzing hardware and software for co-design.
- Interpret co-design prototype required for formal verification and co-simulation.
- Summarize the interfacing of external hardware and software with some examples.

UNIT – I	**8 Hours**

Introduction: The Importance of Embedded Systems, Design of Embedded Systems, The POLIS System.

Models and Representations: Co-design models and languages, CFSMs: Intuitive Semantics.

Text1:1.1, 1.2, 1.3, 2.1, 2.2.

Self-Study Component:	1. Illustrate the importance of Co- Design Issues.

UNIT – II	**8 Hours**

Models and Representations: CFSMs: Mathematical Model, CFSMs: Modelling Data Flow, The SHIFT Format, Specification: Synchronous Languages, Overview of the ESTEREL language, Specification: Graphical FSMs, Modelling Software CFSMs, Software Cost Model, Processor Characterization Model.

Text1:2.3 -2.11.

Self-Study Component:	1. Interpret and present Prototyping and emulation techniques 2. Summarize the future developments in emulation and prototyping architecture specialization techniques.

UNIT – III	**8 Hours**

Synthesis: Partitioning and Architecture Selection, Software Synthesis, Software Cost Estimation, Hardware Synthesis.

Interface Synthesis and The Real-Time Operating System: Interface synthesis, Real-Time Operating System Synthesis, Network-Specific Parts: Interfacing Hardware and Software, Target-Specific Parts: Creating an Abstraction, Scheduling-Specific Parts: Coordinating sw-CFSMs.

Text1: 3.1-3.4, 4.1-4.5.

Self-Study Component:	1. Understand the concepts of Common Parts: Filling the Gaps. 2. Analyze and interpret Schedule Validation

UNIT – IV	**8 Hours**

Verification: Rapid Prototyping, Simulation, Co-simulation using the PTOLEMY environment, Simulation as partitioning support, High-level Co-simulation using VHDL, Formal Verification.

Text1: 5.1-5.6.

Self-Study Component:	1. Analyzing the working of co-design computational

	model. 2. Study and Present Concurrency coordinating concurrent computations.

UNIT – V	**8 Hours**

Interfacing to External Hardware and Software: External Hardware, External Software, Interfacing to an External RTOS.
Design Examples: A Dashboard Controller, An Automotive Bus Controller, A Shock Absorber Controller.
Text1: 6.1-6.3, 7.1-7.3.

Self-Study Component:	1. Analyze and interpret System level specification. 2. Understand and present design representation for system level synthesis.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Apply** the basics of embedded systems to understand the co-design models and their significance.	L2	PO1[L2]
CO2	**Illustrate** the partitioning, abstraction and coordinating hardware and software in co-design.	L2,L3	PO1[L2] & PO4 [L3]
CO3	**Analyze** a co-design prototype **apply**ing formal verification and co-simulation.	L3	PO4[L3]
CO4	**Design** a controller for automotive bus, shock absorber and dash motor by applying the concept of co-design.	L4	PO5[L4]

Text Book(s):

1. FeliceBalarin , MassimilianoChiodo , Paolo Giusto , Harry Hsieh , Attila Jurecska , Luciano Lavagno , ClaudioPasserone , AlbertoSangiovanni-Vincentelli , EllenSentovich , Kei Suzuki , BassamTabbara, **"Hardware-Software Co-Design of Embedded Systems"**, The POLIS Approach by Springer Science+Business Media, LLC. ISBN 978-1-4613-7808-2

Reference Book(s):

1. Jorgen Staunstrup, Wayne Wolf, **"Hardware / Software Co- Design Principles and Practice"**,2009, Springer.
2. De Micheli, Mariagiovanna Sami, Giovanni, **"Hardware / Software Co- Design",** 2002, Kluwer Academic Publishers.

Web and Video link(s):

1. https://youtu.be/Gkp753foAgE.
2. https://youtu.be/6EKpkO6oWWw.

E-Books/Resources:

1. https://link.springer.com/book/10.1007/978-1-4615-6127-9.

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2	2			2	

#3				**2**	
#4					**1**

VLSI and Embedded System Laboratory - I			
Course Code	P22MECEL16	**L-T-P-H : 1-0-2-3**	Credits:2
Contact Period	36 Hrs	**CIE**	50
Exam:	3 Hrs.	**SEE**	50

Course Learning Objectives (CLOs)

After learning all the units of the course, the student is able to:

1. Understand the basic knowledge of how to use CADENCE Tool for VLSI concepts.
2. Analyze the ASIC Design flow.
3. Design and Verify Basic/universal gates using verilog code.
4. Design and Verify combinational and sequential circuits.
5. Design and Verify a testing program for specified conditions using multithread application.
6. Design a POSIX based message queue for communicating between two tasks as per the requirements specified.

Course Content

A.VLSI Digital Design

1. Write Verilog Code for the following circuits and their Test Bench for verification,
   - An inverter, Buffer and Transmission gate
   - Basic/Universal gates
   - Flip flop -RS, D, JK, MS, T
2. Write Verilog code for the following circuits and their Test Bench for verification
   - Carry Ripple Adder
   - Carry LookAhead adder
   - Carry Skip Adder

ASIC-Digital Design Flow

Design the following circuits

1. Write a Verilog Code for 8-bit Booth Multiplication (Radix-4)
2. Write Verilog code for 4/8-bit Magnitude Comparator, Parity Generator,
3. Write Verilog code for 4/8-bit, LFSR, Universal Shift Register
4. 6. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence.

B. Embedded Programming Concepts (RTOS)

1. Create ‘n’ number of child threads. Each thread prints the message “ I’m in thread number ” and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.
2. Implement the multithread application satisfying the following:
   i. Two child threads are crated with normal priority.
   ii. Thread 1 receives and prints its priority and sleeps for 50ms and then quits.
   iii. Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits.
   iv. The main thread waits for the child thread to complete its job and quits.

1. Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.
2. Test the program below using multithread application.
   i. The main thread creates a child thread with default stack size and name

'Child_Thread'.

ii. The main thread sends user defined messages and the message 'WM_QUIT' randomly to the child thread.

iii. The child thread processes the message posted by the main thread and quits when it receives the 'WM_QUIT' message.

iv. The main thread checks the termination of the child thread and quits when the child thread complete its execution.

v. The main thread continues sending the random messages to the child thread till the 'WM_QUIT' message is sent to child thread.

vi. The messaging mechanism between the main thread and child thread is synchronous.

3. Test the program application for creating an anonymous pipe with 512 bytes of size and pass the 'Read Handle' of the pipe to a second process using memory mapped object. The first process writes a message 'Hi from Pipe Server'. The 2nd process reads the data written by the pipe server to the pipe and displays it on the console. Use event object for indicating the availability of data on the pipe and mutex objects for synchronizing the access in the pipe.
4. Create a POSIX based message queue for communicating between two tasks as per the requirements given below:-
   i. Use a named message queue with name 'MyQueue'.
   ii. Create two tasks (Task1 & Task2) with stack size 4000 & priorities 99 & 100 respectively.
   iii. Task 1 creates the specified message queue as Read Write and reads the message present, if any, from the message queue and prints it on the console.
   iv. Task2 open the message queue and posts the message 'Hi from Task2'. Handle all possible error scenarios appropriately.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Program Outcome Addressed (PO #) with BTL**
CO1	**Apply** the knowledge of digital circuit for writing the Verilog model for combinational and sequential circuits and apply multithreading concepts to design and implement concurrent applications in a Linux environment	**PO1(L3),PO 5(L2), PO9(L2)**
CO2	**Analyze** the given digital circuit and develop Verilog model for given digital circuits and also analyze the effects of thread prioritization and scheduling on application performance,	**PO2(L2),PO 3(L2),PO5(L 2),PO9(L2)**
CO3	**Design** and **simulate** Complex Digital Systems, and also analyze the effects of thread prioritization and scheduling on application performance	**PO3, PO5, PO8, (L5)**
CO4	**Analysis** of the **design** for power, timing and area.	**PO2, PO5 (L4)**
CO5	**Develop** State Machines for Sequence Detection and develop robust error handling strategies for multithreaded and multiprocess applications.	**PO3, PO5, PO7, (L5)**

Text Book(s):

1. **"Introduction to Embedded Systems",** Shibu K V, TMH Education Pvt Ltd, Second

reprint, 2010, ISBN(13): 978-0-07-014589-4.
2. **"Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology: Circuit Design, and Process Technology"** Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, CRC Press, ISBN-10: 0-8493-7924-5, ISBN-13: 978-0-8493-7924-6, 2006.

Reference Book(s):

1. **"Digital VLSI Design (RTL to GDS)"**Dr. Adam Teman , Emerging nanoscaled Integrated Circuits and Systems (EnICS) Labs Faculty of Engineering, Bar-Ilan University

E-Books/Resources:

1. https://www.youtube.com/watch?v=RbZ3BXbd6_k&list=PLZU5hLL_713x0_AV_rVbay0pWmED7992G
2. https://www.vlsisystemdesign.com/Clock-Tree-Synthesis-Video-Series.php
3. https://www.udemy.com/course/vlsi-academy-physical-design-flow/

Course Articulation Matrix

CO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2
#1	3				2				2				3	
#2		2	2	2	2				3					
#3			2		3			2						
#4		3			3									3
#5			2		3		2							

SEMESTER II

SYSTEM VERILOG
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – II

Course Code:	**P22MECE22**	**Credits:**	**04**
Teaching Hours/Week (L:T:P):	**4 : 0 : 2**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**52**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Understand the syntax and semantics of SystemVerilog.
- To develop SystemVerilog code for given specifications.
- To analyze and debug SystemVerilog programs.
- To develop test benches for testing SystemVerilog design for specifications.
- To evaluate functional coverage and follow up of the requirements.

UNIT – I	**11 Hours**

SystemVerilog Literal Values and Built-in Data Types: Enhanced literal value assignments, define enhancements, SystemVerilog variables, Using 2-state types in RTL models, Relaxation of type rules, Signed and unsigned modifiers, Static and automatic variables, Deterministic variable initialization, Type casting.
SystemVerilog User-Defined and Enumerated Types: User-defined types, Enumerated types.
Text 1: 3.1-3.9, 4.1, 4.2.

Self-Study Component:	1. Understand the unique facilities of SystemVerilog.
Lab component:	1. Using Enumerated type facility in SystemVerilog develop a code to simulate the operation of a traffic control state machine. 2. Develop a Systemverilog code to simulate and verify the operation of a tristate buffer.

UNIT – II	**10 Hours**

SystemVerilog Arrays, Structures and Unions: Structures, Unions, Arrays, The for each array looping construct, Array querying system functions ,The $bits "size of" system function, Dynamic arrays, associative arrays, sparse arrays and strings.
Text 1: 5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7.

Self-Study Component:	1. Understand the Uses of Enumerated types and strings in SystemVerilog.
Lab component:	1. Using Queue type in SystemVerilog develop a code to simulate the operation of stack/queue for given specifications. 2. Using associative array facilities in SystemVerilog simulate the operation of Virtual memory.

UNIT – III	**10 Hours**

SystemVerilog Procedural Blocks, Tasks and Functions: Verilog general purpose always procedural block, SystemVerilog specialized procedural blocks, Enhancements to tasks and functions.
SystemVerilog Procedural Statements: New operators, Operand enhancements, Enhanced for loops, Bottom testing do while loop, the for each array looping construct.
Text 1: 6.1, 6.2, 6.3, 7.1, 7.2, 7.3, 7.4, 7.5.

Self-Study Component:	1. Understand transaction modeling and ATM in System Verilog. 2. Developing a System Verilog code using Enhanced block names, Statement labels, Enhanced case statements, Enhanced if...else decisions.
Lab component:	1. Using function facilities of SystemVerilog develop a code for simulating ALU and verify its operation through test bench. 2. Using task facility of SystemVerilog develop a code to synthesize given logical functionality, verify its operation through test bench and also comment on synthesizability with respect to return type.

UNIT – IV	**11 Hours**

Basic OOP : Introduction, Think of Nouns-not Verbs, Your First Class, Where to Define a Class ,OOP Terminology , Creating New Objects , Object De allocation , Using Objects , Static Variables vs. Global Variables, Class Methods, Defining Methods Outside of the Class ,Scoping Rules, Using One Class Inside Another, Understanding Dynamic Objects , Copying Objects, Public vs. Local, Straying Off Course, Building a Test bench.

Randomization: What to Randomize, Randomization in SystemVerilog, Constraint Details, Solution Probabilities , Controlling Multiple Constraint Blocks, Valid Constraints, In-line Constraints, The pre_randomize and post_randomize Functions.

Text 2: 5.1-5.18, 6.2-6.9.

Self-Study Component:	**1.** Understand the concept of procedural statements and routines.
Lab component:	1. Using class data types in SystemVerilog develop a code for control register with given specifications and simulate its operation. 2. Using randomization facilities in systemverilog develop a test bench to verify the operation of a given logic design.

UNIT – V	**10 Hours**

Threads and interprocess communication: Working with Threads, Disabling Threads, Interprocess Communication, Events, Semaphores, Mailboxes**,** Building a Test bench with Threads and IPC.

Functional Coverage: Introduction , Coverage Types , Functional Coverage Strategies , Simple Functional Coverage Example , Anatomy of a Cover Group , Triggering a Cover Group , Data Sampling , Cross Coverage , Coverage Options , Parameterized Cover Groups , Analyzing Coverage Data , Measuring Coverage Statistics During Simulation.

Text 2: 7.1-7.7, 9.1-9.7, 9.9-9.11

Self-Study Component:	1. Understand the concepts of Composition, Inheritance, and Alternatives.
Lab component:	1. Develop a SystemVerilog code to illustrate the concept of threads and fork. 2. Develop a SystemVerilog code to create semaphores for controlling the register access.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	***Apply*** the Verilog programming basics to	L2	PO1(L2)

	understand the SystemVerilog data types and language constructs.		
CO2	Using class and randomization elements of SystemVerilog ***Develop*** a test bench for given design	L3	PO3(L3)
CO3	***Develop*** a SystemVerilog code for given design requirements.	L5	PO1(L5)
CO4	***Evaluate*** the functional coverage scope of the test bench theoretically/using tools.	L4	PO4(L4)

Text Book(s):

1. **"SystemVerilog For Design: A Guide to Using SystemVerilog for Hardware Design and Modeling",** Stuart Sutherland Simon Davidmann Peter Flake, Spinger , 2nd edition, ISBN-10: 0-387-33399-1 e-ISBN-10: 0-387-36495-1.
2. **"SystemVerilog for Verification a Guide to Learning the Testbench Language Features**", Chris Spear Synopsys, Inc., 2nd edition, ISBN 978-1-4419-4561-7 ISBN 978-0-387-76530-3 (eBook).

Reference Book(s):

1. **"SystemVerilog for Design",** Sutherland, 2nd edition Springer publications, ISBN 978-0-387-36495-7, 2006.
2. **"SystemVerilog Assertions",** Vijaya Raghavan, Springer publications, ISBN 978-1-4614-7324-4, 2014.

Web and Video link(s):

1. http://www.sunburst-design.com/papers/
2. https://fpga.mit.edu/6205/_static/F23/documentation/1800-2017.pdf

E-Books/Resources:

1. https://verificationguide.com/systemverilog/systemverilog-tutorial/
2. www.ece.uah.edu/~gaede/cpe526/2012 System Verilog Language Reference Manual.pdf

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	**3**				
#2			**3**		
#3	**3**				
#4				**3**	

CMOS MIXED MODE VLSI CIRCUITS

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – II

Course Code:	**P22MECE23**	**Credits:**	**04**
Teaching Hours/Week (L:T:P):	**4 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- To understand the methods and techniques of high-speed IC design.
- To analyse the building blocks of CMOS mixed mode circuits.
- To identify and evaluate the topologies and their related performance parameters for CMOS mixed mode circuits.
- To design individual sub blocks and simple blocks of CMOS mixed mode circuits.
- To develop blocks of CMOS mixed mode circuits for given specifications.

UNIT – I	**8 Hours**

MOS Transistors: Transistor structure, characteristics of MOS transistors, Drain current in the strong inversion approximation, Drain current in the sub threshold region, MOS transistor capacitances, Scaling effects on MOS transistors, Electrical characteristics, Temperature effects, Noise models.

Physical Design of MOS IC's: MOS Transistors, Passive components, Capacitors, Resistors, Inductors.

Text 1: 2.1, 2.2, 3.1, 3.2.

Self-Study Component:	1. Spice models for P-MOS and N-MOS transistors and plot Output characteristics.

UNIT – II	**8 Hours**

Basic Current Reference Circuits: Current mirrors, Simple current mirror, Cascode current mirror, Low-voltage active current mirror, Current and voltage references, Bandgap references, Low-voltage bandgap voltage reference.

CMOS Amplifiers: Differential amplifier, Linearization techniques for transconductors, Single-stage amplifier, Folded-cascode amplifier.

Text 1: 4.1, 4.2, 4.2.1, 4.2.2, 4.2.2.1, 5.1-5.4.

Self-Study Component:	1. Design and Simulate current mirrors in CAD tool. Understand the requirements of Op-Amps and their implications on design by referring different vendors' product data sheets

UNIT – III	**8 Hours**

CMOS Amplifiers: Fully differential amplifier architectures, Multi-stage amplifier structures, Amplifier characterization.

Non-Linear Analog Components: Comparators.

Text 1: 5.5, 5.6, 5.6.1- 5.6.3, 5.8, 5.8.1-5.8.3, 5.8.5, 5.8.6, 6.1.

Self-Study Component:	1. Design and simulate a single stage /differential amplifier for given requirements across different technologies, note the limitations and benefits.

UNIT – IV	**8 Hours**

Switched Capacitor Circuits: Anti-aliasing filter, Capacitors, Switches, Programmable capacitor arrays, Operational amplifiers, Track-and-hold (T/H) and sample-and-hold (S/H)

circuits, Switched-capacitor (SC) circuit principle, SC filter design, SC ladder filter based on the LDI transform, Effects of the amplifier finite gain and bandwidth,
Text 1: 8.1-8.9, 8.11.

Self-Study Component:	**1.** To study and understand "Dynamic analog resonator-based adaptive filters". ISCAS 2000: 161-164 IEEE International Symposium on Circuits and Systems, May 28-31, 2000, Geneva, Switzerland.

UNIT – V	**8 Hours**

Data Converter Principles: Data converter characterization. **Nyquist Digital-to-Analog Converters:** Digital-to-analog converter (DAC) architectures, Voltage-scaling DACs, Configuring a unipolar DAC for the bipolar conversion. **Nyquist Analog-to-Digital Converters:** Analog-to-digital converter (ADC) architectures.
Text 1: 9.2, 10.1, 10.2, 10.3, 11.1, 11.1.1.

Self-Study Component:	1. To study IEEE Transaction article "A high-frequency double-sampling second-order DeltaSigma modulator" and simulate any functional block.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Apply**ing the fundamentals of semiconductor theory for understanding the MOS device physics and its modes	**L2**	**PO1 [L2]**
CO2	**Analyze** the MOSFET based current mirrors, voltage reference circuits, differential amplifiers and its applied circuits along with the switched capacitors circuits	**L3**	**PO1, PO4 [L3]**
CO3	**Design** MOSFET based current mirrors, amplifiers and switched capacitor filters for given specifications	**L4**	**PO4[L4]**
CO4	**Interpret** and **discuss** the principles and working mechanism of different MOSFET based analog to digital convertors and digital to analog convertors	**L3**	**PO1[L3]**
CO5	**Develop** MOSFET based circuit for given application of filtering or amplifiers or reference voltage generalizations	**L4**	**PO4, PO5[L4]**

Text Book(s):
1. **"CMOS Analog Integrated Circuits High-Speed and Power-Efficient Design",**Tertulien Ndjountche, CRC Press, ISBN: -13: 978-1-138-59972-7, 2019.

Reference Book(s):
1. **"Design of Analog CMOS Integrated Circuits**", Behzad Razavi, Tata McGraw Hill, 1st edition, ISBN 0-07-238032-2, 2008.
2. **"CMOS Analog Circuit Design",** Phillip E. Allen, Douglas R.Holberg, Oxford University Press, 3rd edition, ISBN: 9780199765072, 2011.
3. **"CMOS Circuit Design, Layout and Simulation",** R. Jacob Baker,Harry W. Li, David E. Boyce, Prentice Hall of India, 1st edition, ISBN-13: 978-0780334168 ISBN-10: 0780334167, 2005.

Web and Video link(s):

1. https://www.youtube.com/playlist?list=PL_uaeekrhGzIDoH9oXE_xiG2k0rpioWlN
2. https://cmosedu.com/

E-Books/Resources:

1. https://www.amazon.in/CMOS-Analog-Integrated-Circuits-Power-Efficient/dp/0367733293
2. https://www.routledge.com/CMOS-Analog-Integrated-Circuits-High-Speed-and-Power-Efficient-Design-Second-Edition/Ndjountche/p/book/9780367733292#:~:text=Description,%2C%20instrumentation%2C%20and%20control%20systems.
3. https://ioe.iitm.ac.in/project/rf-analog-and-mixed-signal-integrated-circuits

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2		2		3	
#3				3	
#4	2				
#5				1	1

Professional Elective –III

ARM PROCESSORS [As per Choice Based Credit System (CBCS) & OBE Scheme] **SEMESTER – II**			
Course Code:	**P22MECE241**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Understand the technical overview of Cortex-M processor.
- Recognize the ARM processor's overall architecture.
- Implement embedded systems using Cortex M3 & M4
- Know what control registers are all about.
- Analyse the faults and exceptions in ARM Processor.

UNIT – I	**8 Hours**

Introduction to ARM Cortex-M Processors: What are the ARM Cortex-M processors? Advantages of the Cortex-M processors.
Technical Overview: General information about the Cortex-M3 and Cortex-M4 processors, Features of the Cortex-M3 and Cortex-M4 processors
Text1: 1.1, 1.2, 3.1, 3.2

Self-Study Component:	1. Applications of the ARM Cortex-M processors. 2. Resources for using ARM processors and ARM microcontrollers

UNIT – II	**8 Hours**

Introduction to the architecture: Architecture, Programmer's model, Behavior of the application program status register (APSR), Memory system, Exceptions and interrupts
Memory systems: Overview of memory system features, Memory map, Connecting the processor to memory and peripherals, Memory requirements, Memory endianness.
Text1: 4.1, 4.2, 4.3, 4.4, 4.5, 6.1, 6.2, 6.3, 6.4, 6.5

Self-Study Component:	1. System control blocks (SCB). 2. Bit band operations.

UNIT – III	**8 Hours**

Exceptions and Interrupts: Overview of exceptions and Exception types, Overview of interrupt management, Definitions of priority, Vector table and vector table relocation, Interrupt inputs and pending behaviors, Exception sequence overview, Details of NVIC registers for interrupt control, Details of SCB registers for exception and interrupt control.
Text1: 7.1-7.9

Self-Study Component:	1. Special registers for exception or interrupt masking. 2. Procedures in setting up interrupts.

UNIT – IV	**8 Hours**

Low Power and System Control Features: Low power designs, Low power features, Using WFI and WFE instructions in programming, CPU ID base register, Configuration control register, Auxiliary control register, Co-processor access control register
Memory Protection Unit (MPU): Overview of the MPU, MPU registers, Setting up the MPU, Memory barrier and MPU configuration, Using sub-region disable.
Text1: 9.1, 9.2, 9.3, 9.7, 9.8, 9.9, 9.10,11.1, 11.2, 11.3, 11.4, 11.5

Self-Study Component:	1. SysTick Timer. 2. Other usages of the MPU

	3. Comparing with the MPU in the Cortex-M0+ processor

UNIT – V	**8 Hours**

Fault Exceptions and Fault Handling: Overview of fault exceptions, Enabling fault handlers, Fault status registers and fault address registers, Analyzing faults, Faults related to exception handling, Lockup, Fault handlers.
Introduction to the Debug and Trace Features: Debug and trace features overview, Debug architecture, Debug modes, Debug events.
Text 1: 12.1-12.8, 14.1-14.4.

Self-Study Component:	1. Concepts of Running a system with two stacks and Detect stack overflow 2. Debug components introduction and its operation.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Understand** the fundamentals of ARM Cortex-M processors and their various types.	L2	PO1 [L2]
CO2	**Illustrate** the applications of Cortex-M3 and Cortex-M4 processors in real-world scenarios.	L2	PO1 [L2]
CO3	**Implement** interrupt management techniques, such as defining priorities and relocating vector tables, in embedded system designs using ARM Cortex-M processors.	L3	PO2 [L3]
CO4	**Analyze** how different memory configurations affect system performance.	L4	PO3 [L4]
CO5	**Build** simple Embedded Applications using Input and output devices with ARM core and a controller	L5	PO5 [L5]

Text Book(s):
1.Joseph Yiu **"The Definitive Guide to ARM_ Cortex_-M3 and Cortex-M4 Processors"**, 3rd edition, Newness publications, 2016**,** ISBN13: 978-0-12-408082-9

Reference Book(s):
1.Steve Furber **"ARM System –On-Chip-Architecture"**, 2nd Ed, Addison Wesley
2.Andrew Sloss, Dominic Symes, Chris Wright **"ARM System Developer's Guide: Designing and Optimizing System Software** ". Elsevier Morghan Kaufmann publishers ISBN 1-55860-874-5

E-Books/Resources:
1.https://www.google.co.in/books/edition/The_Definitive_Guide_to_ARM_Cortex_M3_an/9YxqAAAAQBAJ?hl=en&gbpv=1&dq=1.%09Joseph+Yiu+%E2%80%9CThe+Definitive+Guide+to+ARM+Cortex-M3+and+Cortex-M4+Processors%E2%80%9D,+3rd+edition,+Newness+publications,+2016,+ISBN13:+978-0-12-4080+82-9&printsec=frontcover

Course Articulation Matrix (CAM)					
CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**
#1	**3**				
#2	**2**				
#3		**3**			
#4			**2**		
#5					**2**

EMBEDDED SYSTEM DESIGN WITH FPGA

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – II

Course Code:	P22MECE242	**Credits:**	03
Teaching Hours/Week	3 : 0 : 0	**CIE Marks:**	50
Total Number of Teaching Hours:	40	**SEE Marks:**	50

Course Learning Objectives (CLOs)

After learning all the units of the course, the student is able to

1. Provides basic knowledge of embedded system.
2. Explain the computer hardware and software.
3. Illustrate the concept of the SAYEH Design and Test.
4. Describe the concept of Field Programmable gate arrays.
5. Explain the embedded system design tools and design protyping.
6. Describe the various concept of design of utility hardware cores.

UNIT – I	**8 Hours**

Computer Hardware and Software: Computer System, Computer Software, Machine Language, Assembly Language, High-Level Language, C Programming Language, Instruction Set Architecture, SMPL-CPU Design, CPU Specification, Single-Cycle Implementation, , SAYEH Design and Test, Details of Processor Functionality, SAYEH Datapath, SAYEH Verilog Description, SAYEH Top-Level Testbench / Assembler. **Text 1 :4.1-4.5.**

Self-Learning Component:	Multi-Cycle Implementation, SAYEH Hardware Realization.

UNIT – II	**8 Hours**

Field Programmable Devices: Read Only Memory, Basic ROM Structure, NOR Implementation, Distributed Gates, Array Programmability, Memory View, ROM Variations, Programmable Logic Arrays, PAL Logic Structure, Product Term Expansion, Three-State Outputs, Registered Outputs, Complex Programmable Logic Devices, Altera's MAX 7000S CPLD, Field Programmable gate arrays, Altera's FLEX 10K DOGMA, Altera's cyclone DOGMA.

Text 1: 5.1-5.4.

Self-Learning Component:	Commercial Parts, Altera's cyclone DOGMA.

UNIT – III	**8 Hours**

Tools For Design and Prototyping: Hardware Design Flow, Datapath of Serial Adder, Serial Adder Controller, HDL Simulation and Synthesis, Pre-Synthesis Simulation, Module Synthesis, Post-Synthesis Simulation, Mixed-Level Design with Quartus II, Project Specification, Block Diagram Design File, Creating and Inserting Design Components, Wiring Design Component, Design Compilation, Design Simulation, Synthesis Results, Design Prototyping, UP3 Board Specification,

Text 1:6.1-6.4.

Self-Learning Component:	DE2 Board Specification, Programming DE2 Cyclone II.

UNIT – IV	**8 Hours**

Design of Utility Hardware Cores: Library Management, Basic IO Device Handling, Debouncer, Single Stepper, Utilizing UPS Basic IO, Utilizing DE2 Basic IO, Frequency Dividers, Seven Segment Displays, SSD Driver, Testing DE2 SSD Driver, LCD Display

Adapter, Writing into LCD, LCD Initialization, Display Driver with Initialization, Testing the LCD Driver (UPS), Testing the LCD Driver (DE2), Keyboard Interface Logic, Serial Data Communication, Power-On Routine, Codes and Commands, Keyboard Interface Design, VGA Interface Logic, VGA Driver Operation, Monitor Synchronization Hardware, Character Display, VGA Driver for Text Data, VGA Driver Prototyping (UPS),.

Design with Embedded Processors: Embedded Design Steps, Processor Selection, Processor Interfacing, Developing Software, Filter Design, Filter Concepts, FIR Filter Hardware Implementation, FIR Embedded Implementation, Building the FIR Filter, Design of a Microcontroller, System Platform.

Text 1: 7.1-7.7,8.1-8.3.

Self-Learning Component:	Design of Calculating Engine, Building Calculator Software, Calculator Program, Completing the Calculator System.

UNIT – V	**8 Hours**

Design Of An Embedded System: Designing an Embedded System, Nios II Processor, Configurability Features of Nios II, Processor Architecture, Instruction Set,Nios II Alternative Cores, Avalon Switch Fabric, Avalon Specification, Address Decoding Logic, Data-path Multiplexing, Wait-state Insertion, Pipelining, Endian Conversion, Native Address Alignment and Dynamic Bus Sizing, Arbitration for Multi-Master Systems, Burst Management, Clock Domain Crossing, Interrupt Controller, Reset Distribution, SOPC Builder Overview, Architecture of SOPC Builder Systems, Functions of SOPC Builder, IDE Integrated Development Environment, IDE Project Manager, Source Code Editor, C/C++ Compiler, Debugger , Flash Programmer, An Embedded System Design: Calculator, System Specification, Calculating Engine, Calculator IO interface.

Text1: **9.1-9.6.**

Self-Learning Component:	Calculator Program, Completing the Calculator System, Design of Calculating Engine, Building Calculator Software.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Apply**the knowledge ofMachine Language, Assembly Language, High LeveI Language.	Apply	PO1,[L2]
CO2	**Analyze** the concept of SAYEH Top-Level Testbench / Assembler.	Analyze	PO2 [L3]
CO3	**Develop**the FIR Filter Hardware and Embedded Implementation.	Create	PO3 [L4]
CO4	**Design and develop** the Calculator, Calculating Engine and Calculator IO interface.	Create	PO3[L4]

Text Book(s):

1. **"Embedded Core Design with FPGAs"**, ZainalabedinNavabi, First edition, McGraw Hill, ISBN-10: 0070139784, ISBN-13: 978-0070139787, 2008.

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2		3			
#3			3		
#4			3		

ROBOTICS AND AUTOMATION

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – 11

Course Code:	**P22MECE243**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Familiarize the history of robot and basic concepts of industrial robot.
- Illustrate kinematics of robots and programming of robot.
- Understand and analyze the trajectory planning for robot.
- Analyze Euler, Lagrangian formulation of Robot dynamics
- Summarize the various applications of robots in modern automation industry.

UNIT – I	**8 Hours**

Introduction: Industrial Automation and Computers, Industrial Robot, Robot Population and Application, Do Robots Create More Unemployment? Payback Period of a Robot, Robot Applications in Manufacturing

Grippers and Tools of Industrial Robot: Introduction, Definitions of Industrial Robot, Configuration and Work Volume, Precision of Movement, Degrees of Freedom, End Effectors.

Coordinate Transformation: Introduction, 2D Coordinate Transformation, Description of Object, 3D Coordinate Transformation.

Text 1: Chapter 2.

Self-Study Component:	1. Understand the coordinate frames and transformations using Robot Analyzer. 2. Demonstrate the components and applications of industrial Robot.

UNIT – II	**8 Hours**

Coordinate Transformation: Inverse Transformation, Composite Transformation Matrix, The Wrist.

Kinematics: Introduction, Joint Coordinate Space, Kinematics and Inverse Kinematics, Link Parameters, D-H Notation of Coordinate Frames, D-H Transformation Matrix, Symbolic Procedure, D-H Algorithm, Application Examples, Jacobian.

Text 1: Chapter 3.5-3.7, Chapter 4

Self-Study Component:	1. Study and present forward kinematics and validation using modern tool (RoboAnalyser/Matlab or any other free software tool). 2. Demonstrate kinematics of an industrial robot and validation using any open source software or simpler laboratory version of robotic arm.

UNIT – III	**8 Hours**

Robot Sensors: Introduction, Internal and External Sensors, Applications of Robot Sensors, Desirable Features of Robot Sensors, Proximity and Tactile Sensors, Range Sensors, Force Sensors.

Robot Control: Introduction, Euler–Lagrange Equation, Joint Motion, Second-Order Systems, Lyapunov Stability, Lyapunov First Method, Lyapunov Second Method, Control Unit, Electric, Hydraulic and Pneumatic Drives, Industrial Vision System, Inspection Using Industrial Vision, Camera.

Text 1: Chapter 5.1-5.7, 6.1-6.4,6.6-6.13.

Self-Study Component:	1. Study Vision system for inspection of robot sensor and state space equation on robot control.

	2. Illustrate the concept of Integration of assorted sensors (IR, Potentiometer, strain gages etc.) to micro controllers.

UNIT – IV	**8 Hours**

Robot Programming and Work Cell: Introduction, Language Structure, Robot Programming Languages, Robot Motion, SCORBOT-ER, Sensor Integration, Robot Work Cell, Interference Problems, Interference Problems, Further on Robot Work Cell.
Robot Trajectory Planning: Introduction, Trajectory Planning Terminologies, Steps in Trajectory Planning, p-Degree Polynomial Trajectories, Linear Function with Parabolic Blends, Issues on LFPB Trajectories, Bang-Bang Trajectory, Cartesian Space Versus Joint Space.
Text 1: chapter 7, 10

Self-Study Component:	1. Develop a program in VAL II to command a PUMA robot to unload a cylindrical part of 10 mm diameter from machine 1 positioned at point P1 and load the part on machine 2 positioned at P2. The speed of robot motion is 40 in./s. However, because of safety precautions, the speed is reduced to 10 in./s while moving to a machine for an unloading or loading operation. 2. Demonstrate Denavit-Hartenberg (DH) parameter validation using Robo Analyser software.

UNIT – V	**8 Hours**

Robot Dynamics: Introduction, Lagrangian Design, N-Link Robot Manipulator, Slender Rod as Robot Link.
Robot Applications: Robots in Industry, Robots in Handling, Compliance, Assembly, Injection Moulding.
Medical Applications of Robots: Classification of Medical Robots, Slow Growth, Rehabilitation Robots, Guide Robot, Guide Cane, Prosthetic Limb, Prosthetic Arms, Exoskeleton, Hospital Service Robot, Clinical Robot
Text 1: Chapter 13, 9,15

Self-Study Component:	1. Illustrate the concept of Electronic sensor based navigation aids. 2. Case study on Robotics in healthcare and present the report on future of robots in medicine.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Analyze** various robots, end effectors, applications, and operational workspace.	L3	PO3[L3]
CO2	**Apply** spatial transformation to obtain forward kinematics and inverse kinematics equation of robot manipulators.	L2	PO3[L2]
CO3	**Analyze** the operations of various sensors, actuators and controller for **design**ing Robotic applications.	L4	PO3,PO5[L4]
CO4	**Understand** the use of VAL II programming commands and develop a program to control robotic movements.	L2,L3	PO1,PO5[L2,L3]

Text Book(s):

1. Ramachandran Nagarajan,**"Introduction to Industrial Robotics"**, Pearson, 2016 ISBN 978-93-325-4480-2, e-ISBN 978-93-325-7872-2.

Reference Book(s):

1. S K Saha, **"Introduction to Robotics"**, McGraw Hill, 2014 ISBN (13): 978-93-3290-280- 0,ISBN (10): 93-3290-280-1.
2. Michell Grover, Mitchel weiss, Roger nagel, **"Industrial Robots"**, McGraw Hill 2012, India ,2ND edition, ISBN-13:9780070265097.
3. K.S. Fu, R.C. Gonzales and Lee, **"Robotics"**, McGraw Hill Intl. India, 1ST edition, 2008 ISBN-13:9780070265103.
4. Yoramn Koren, **"Robotics for Engineers"**, McGraw hill Intl. Book Co., New Delhi 1987, ISBN-13:9780070353992.

Web and Video link(s):

1. https://archive.nptel.ac.in/courses/112/105/112105249/.
2. http://nitttrc.edu.in/nptel/courses/video/112105249/L31.html.

E-Books/Resources:

1. https://libgen.rocks/ads.php?md5=90f7c33400ed39a1c4d63e50de1c2671.

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1			3		
#2			3		
#3			2		2
#4	1				2

ADVANCED in VLSI SYSTEM

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – II

Course Code:	**P22MECE244**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Provide the basic knowledge of Advances in VLSI Design.
- Explain the concept of MOS, CMOS, BiCMOS, MESFET and MODFET operations.
- Provide the understanding of MIS Structures and MOSFETS.
- Highlight the concept of Short Channel Effects and Challenges to CMOS.
- Provide the knowledge of Evolutionary advances beyond CMOS.
- Explain the concept of Super Buffers, Bi-CMOS and Steering Logic.

UNIT – I	**8 Hours**

Review of MOS Circuits: MOS and CMOS static plots, switches, comparison between CMOS and Bi - CMOS.

MESFETS: MESFET and MODFET operations, quantitative description of MESFETS

Text 1: 5.2, 5.3.

Self-Study Component:	Small Signal model for a MESFETs

UNIT – II	**8 Hours**

MIS Structures and MOSFETS: MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.

Short Channel Effects and Challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization.

Text 1: 6.1-6.4, 7.1-7.3.

Self-Study Component:	CMOS circuits analysis

UNIT – III	**8 Hours**

Beyond CMOS: Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode-diode logic .Defect tolerant computing,

Text 1: 8.1-8.5.

Self-Study Component:	Quantum dot cellular automata

UNIT – IV	**8 Hours**

Super Buffers, Bi-CMOS and Steering Logic: Introduction, RC delay lines, super buffers-An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks.

Text 2: Chapter 6

Self-Study Component:	CMOS super buffer Applications

UNIT – V	**8 Hours**

Special Circuit Layouts and Technology Mapping: Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module lay out.

System Design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, Programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom Design

Text 3: 14.2, 14.3.3, 14.3.5.

Self-Study Component:	Perform Platform Based Design.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Describe** the basic operation and characteristics of CMOS, Bi-CMOS, MISFETS, MESFET and MODFET devices.	L2	PO1 [L2]
CO2	**Analyze** the short channel effects and challenges in CMOS devices.	L4	PO1,PO4 [L4]
CO3	**Discuss** about the advancement in the CMOS device technology.	L2	PO1 [L2]
CO4	**Analyze** the working of Super Buffers, Bi-CMOS and Steering Logic circuits.	L4	PO1 [L4]
CO5	***Design*** **and** ***Analyze*** the different concepts of special circuit layouts and system design along with design constraints.	L4,L6	PO1 [L4,L6]

Text Book(s):

1. Kevin F Brrnnan "**Introduction to SemiConductor Device**", Cambridge publications, ISBN 10: 0-521-15361-1, ISBN 13:978-0-521-153614.
2. Eugene D Fabricius "**Introduction to VLSI Design**", McGraw-Hill International publications, ISBN 10: 0070199485, ISBN 13:978-0070199484.
3. Neil H. E. Weste, David Money Harris, **"CMOS VLSI Design: a Circuits and Systems Perspective",** Pearson, 4th edition, ISBN 10: 0-321-54774-8, ISBN 13:978-0-321-54774.

Reference Book(s):

1. Wayne Wolf, "Modern VLSI Design" Pearson Education, 3th Edition,ISBN 10: 8178086530, ISBN 13:978-8178086538.
2. Jan M Rabey, Anantha Chandrakasan, Borivoje Nikolic, —"Digital Integrated Circuits-A Design Perspective‖", PHI, 2nd Edition, ISBN 10: 9385152343, ISBN 13:978-9332573925.

Web and Video link(s):

1. https://youtu.be/VAStNe9s1s8?si=htdm9wWyvHbLlWYX
2. https://youtu.be/XGzs8gID7SY?si=sURUTpqk9WsgdGtk
3. https://youtu.be/K0CAvBnSAI4?si=zmsgRbHX-jWIPMHa

E-Books/Resources:

1. https://assets.cambridge.org/97805218/31505/frontmatter/9780521831505_frontmatter.pdf
2. https://dokumen.pub/cmos-vlsi-design-a-circuits-and-systems-perspective-4th-edition-0321547748-9780321547743.html

Course Articulation Matrix (CAM)					
CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**
#1	**2**				
#2	**2**			**2**	
#3	**2**				
#4	**2**				
#5					

Professional Elective –IV

LOW POWER VLSI DESIGN [As per Choice Based Credit System (CBCS) & OBE Scheme] **SEMESTER – II**			
Course Code:	**P22MECE251**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: At the end of the course will enable the students to:

- Understand the types of power dissipation in CMOS devices.
- Discuss different techniques of power analysis and digital cell library.
- Discuss the concepts of Low power Clock Distribution.
- Design low power arithmetic circuits and systems.
- Understand the architecture and performance management of the system.

UNIT – I	**8 Hours**

Introduction: Needs for Low Power VLSI Chips, Charging and Discharging Capacitance, Short-circuit Current in CMOS Circuit, CMOS Leakage Current, Basic Principles of Low Power Design, Low Power Figure of Merits.

Simulation Power Analysis: SPICE Circuit Simulation, Discrete Transistor Modeling and Analysis, Gate-level Logic Simulation, Architecture-level Analysis.

Text 1: 1.1-1.4, 1.6, 1.7, 2.1-2.4.

Self-Study Component:	1. Understand the influence of Static Current in power analysis. 2. Understand how the Data Correlation Analysis is done in DSP Systems

UNIT – II	**8 Hours**

Probabilistic Power Analysis: Random Logic Signals, Probability and Frequency, Probabilistic Power Analysis Techniques.

Circuit: Transistor and Gate Sizing, Equivalent Pin Ordering, Network Restructuring and Reorganization, Adjustable Device Threshold Voltage.

Text 1:3.1-3.3, 4.1-4.3, 4.6.

Self-Study Component:	1. Discuss the concept of Signal Entropy 2. Discuss the concept of Low Power Digital Cell Library.

UNIT – III	**8 Hours**

Low Power Circuit Techniques: Introduction, Power Consumption in Circuits, Flip-flops and Latches, Logic.

Power Clock Distribution: Power Dissipation in Clock Distribution, Single Driver vs. Distributed Buffers**,** Buffer and Device Sizing under Process Variations, Zero Skew vs. Tolerable Skew.

Text 2: 3.1- 3.4, 5.1- 5.4.

Self-Study Component:	1. Understand the concept of High Capacitance Nodes. 2. Explain how the Chip and Package Co-Design of Clock Network is done.

UNIT – IV	**8 Hours**

Low Power Arithmetic Components: Introduction**,** Circuit Design Style**,** Adders, Multipliers.

Low Power Memory Design: Introduction, Sources and Reductions of Power Dissipation in Memory Subsystem, Sources of Power Dissipation in SRAM.

Text 2: 7.1- 7.4, 8.1 - 8.3.

Self-Study Component:	1. Understand the concept of division in low power arithmetic components. 2. Compare the features of Low Power SRAM and DRAM Circuits.

UNIT – V	**8 Hours**

Architecture and System: Power and Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction, Operator Reduction.
Advanced Techniques: Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous System Basics.
Text 1: 7.1-7.4.1, 8.1-8.3.1.

Self-Study Component:	1. Understand the concept of Loop Unrolling. 2. Understand the concept of Prospects of Asynchronous Computation.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	Analyze the basic knowledge of fundamental circuit concept and need of low power VLSI circuits.	L4	PO2
CO2	Estimate and illustrate the power dissipation in VLSI circuits	L3	PO3
CO3	Understand the probabilistic power using different technique.	L2	PO1
CO4	Apply basic understanding different low power techniques for combinational circuits and memory design.	L3	PO3

Text Book(s):

1. "Practical Low Power VLSI Design", Gary K, Yeap, Kluwer Academic Publishers, ISBN – 13: 978-0792380092, 2008,
2. "Low Power Design Methodologies" Rabaey, Pedram, Kluwer Academic Publishers, ISBN – 978-1-4613-5975-3, 2009.

Reference Book(s):

1. **"Low Power Low Voltage VLSI Subsystem"** Kiat Seng Yeo and Kausik Roy**,** Tata Mc Gram Hill. ISBN-9780071437868, 2005.
2. **"Designing CMOS Circuits for Lower Power"** Soudris D, Piguet C and Goutis C, Kluwer Academic Publishers, ISBN -9781402072345, 2002.

Web and Video link(s):

1. https://www.youtube.com/watch?v=TFOO1JAll2Y
2. https://www.youtube.com/watch?v=aRXd1M6bo2w
3. https://www.youtube.com/watch?v=XoHkE4xgaFA.

E-Books/Resources:

1. https://archive.org/details/lowvoltagelowpow0000yeok.
2. https://www.google.co.in/books/edition/Low_Power_Cmos_Vlsi_Circuit_Design/eQKCHEyJcewC?hl=en&gbpv=0.

Course Articulation Matrix (CAM)					
CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**
#1	**3**	**2**			
#2			**2**		
#3	**3**				
#4			**2**		

AUTOMOTIVE ELECTRONICS

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – II

Course Code:	**P22MECE252**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Understand the concepts of Automotive Electronics and its evolution and trends.
- Illustrate the various application of electronics systems and ECU in automotive.
- Describe principles and applications of sensors and actuators in automotive electronics systems.
- Summarize the various control systems and communication protocols in automotive.
- Illustrate the modern advanced technologies and trends in automotive.

UNIT – I	**8 Hours**

Basic Fundamental: Electrical and electronic systems in the vehicle, Overview, Lighting technology, electronic stability program (ESP), Adaptive cruise control (ACC).

Basic Principles of Networking: Network topology, Network organization, OSI reference model, Control mechanisms.

Automotive Networking: Cross-system functions, Requirements for bus systems, Classification of bus systems, Applications in the vehicle, Coupling of networks, Examples of networked vehicles.

Text 2.

Self-Study Component:	1. Study the basic fundamentals of automotive systems. 2. Explore Automotive Networking in different Application.

UNIT – II	**8 Hours**

The Basic of Electronic Engine control: Motivation for Electronic Engine Control, Exhaust Emissions, Fuel Economy, Federal Government Test Procedures, and Concept of an Electronic Engine control system, Definition of Engine performance terms, Exhaust Catalytic Converters, Electronic Fuel control system, Analysis of intake manifold pressure, Idle Speed Control, Electronic Ignition.

Text 1: Chapter 4.

Self-Study Component:	1. Study the basic functioning of electronic engines. 2. Compare different types of electronic ignition.

UNIT – III	**8 Hours**

Automotive Sensor: Airflow rate sensor, Engine Crankshaft Angular Position Sensor, Magnetic Reluctance Position Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle Angle Sensor (TAS), Engine Coolant Temperature (ECT) Sensor, Knock Sensor.

Text 1: Chapter 5.

Automotive Actuators: Electromechanical actuators, Fluid-mechanical actuators, Electrical machines.

Text 2.

Self-Study Component:	1. Study and present angular rate sensors and flex-fuel sensors in automotive applications. 2. Explore automotive engine control actuators.

UNIT – IV	**8 Hours**

Digital Powertrain Control Systems: Introduction, Digital Engine control, Control modes for fuel Control, Discrete Time Idle Speed Control, EGR Control, Variable valve timing control, Direct Fuel Injection, Flex Fuel, Electronic Ignition Control, Integrated Engine Control System, Secondary Air Management, Evaporative Emissions Canister Purge, Automatic System Adjustment, System Diagnostics.
Text 1: Chapter 6
Control Units: Operating conditions, Design, Data processing, Digital modules in the Control unit, Control unit software.

Self-Study Component:	1. Explore designing engine control systems. 2. Illustrate programmable control units in automotive systems.

UNIT – V	**8 Hours**

Vehicle Communications: IVN, CAN, Local Interconnect Network, FlexRay IVN, MOST IVN, Vehicle to Infrastructure Communication, Vehicle-to-Cellular Infrastructure, Quadrature Phase Shifter and Phase Modulation (QPSR), Short-Range Wireless Communications, Satellite Vehicle Communication, GPS Navigation.
Electronic Safety-Related Systems: Airbag Safety Device, Blind Spot Detection, Automatic Collision Avoidance System.
Autonomous Vehicles: Automatic Parallel Parking System, Autonomous Vehicle Block Diagram.
Text 1: Chapter 9, Chapter 10 and Chapter 12.

Self-Study Component:	1. Study of Electronic Control System Diagnostics. 2. Distinguish Lane Departure Monitor and Tire Pressure Monitoring System.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Interpret** an overview of automotive components, subsystems and basics of Electronic Engine Control in modern automotive sector.	L2	PO1[L2]
CO2	Apply the concepts of automotive sensors and actuators in various electronic control systems to design of automotive system.	L5	PO4[L5]
CO3	Analyze and Illustrate the networking concepts in various modules of automotive systems and communication protocols for interfacing electronics components, systems and mechanical parts.	L2, L3	PO1[L2] & PO5[L3]
CO4	**Analyze** the various automotive control systems and Safety-Related Systems.	L3,L4	PO4[L3] & PO5[L4]

Text Book(s):

1. William B. Ribbens, **"Understanding Automotive Electronics"**, 8th Edition, Elsevier Publishing. ISBN: 9780128104347.
2. Robert Bosch Gmbh (Ed.) **"Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive"**, 5th edition, John Wiley& Sons Inc., 2007. ISBN: 3658017848, 9783658017842.

Reference Book(s):

1. Nazamuz Zaman, **"Automotive Electronics Design Fundamentals"**, 2015, Springer Publications. ISBN: 978-3-319-17584-3.

Web and Video link(s):

1. https://youtu.be/BOP8qLQzhDc.
2. https://youtu.be/hs7bABMtOMI.
3. https://youtu.be/zzpOtJA-Rqw.

E-Books/Resources:

1. https://www.elsevier.com/books/understanding-automotive-electronics/ribbens/978-0-12-810434-7.
2. https://www.academia.edu/42742205/Bosch_Professional_Automotive_Information.

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2				2	
#3	3				2
#4				2	1

DESIGN OF VLSI SYSTEM

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – II

Course Code:	**P22MECE253**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Provide the basic knowledge of VLSI system design.
- Explain the concept of VLSI System Design Methodology and Chip Design Methods.
- Provide the understanding of Design Capture Tools.
- Highlight the concept of Data Path Sub System Design and Array Subsystem Design
- Outline the concepts of Control Unit Design and Special Purpose Subsystems.
- Provide the knowledge of Design Economics, VLSI System Testing & Verification.

UNIT – I	**8 Hours**

VLSI Design Methodology: Introduction, Structure Design Strategies: Hierarchy, Regularity, Modularity, and Locality. System on Chip Design options: Programmable logic and structures, Programmable interconnect, Programmable gate arrays, Sea of gate and gate array design, standard cell design, full custom mask design and Platform based design – system on a chip.

Design Flows: Behavioral synthesis, RTL synthesis, Logic optimization and structural tools layout synthesis, layout synthesis, EDA Tools for System.

Text 2: 14.1, 14.2, 14.3, 14.4.

Self-Study Component:	3. Layout Design and Tools: Hierarchical Stick Diagrams, Automatic Layout.

UNIT – II	**8 Hours**

Design Capture Tools: HDL Design, Schematic Design, Layout Design, Floor planning and Chip Composition. Design Verification Tools: Simulation Timing Verifiers, Net List Comparison Layout Extraction, Design Rule Verification.

Text 1:

Self-Study Component:	3. Design Rules: Scalable Design Rules, Fabrication Errors and Typical Process Parameters.

UNIT – III	**8 Hours**

Datapath Subsystem Designs: Basic Combinational Components: Decoders, Encoders, Multiplexers, Demultiplexers and Magnitude Comparators.

Basic Sequential Component: Registers, Shift Registers, Counters, and Sequence generators. Shifters, Addition/ Subtraction, Parallel prefix adders, Multiplication: Signed and Unsigned Multipliers and Division.

Memory Subsystems: Introduction: Memory Classification, Memory organization and Memory access timing. Static Random Access Memory (SRAM): RAM Core Structures, Operations of SRAM, Row decoders, Column decoders / Multiplexers, and Sense amplifiers. Dynamic Random Access Memory (DRAM): Cell structures, Structures of Memory array, Read only Memory. Nonvolatile Memory: Flash Memory, other Nonvolatile Memories. Other Memory Devices: Content Addressable Memory, Register files, Dual port RAM.

Text 1: 10.1-10.6, 11.1-11.6.

Self-Study Component:	3. Case study for different types of adder, shifter and multiplier, Programmable logic arrays and FIFO.

UNIT – IV	**8 Hours**

Power Distribution and Clock Designs: Power Distribution Networks: Design issues of power distribution networks and Power distribution networks. Clock Generation and Distribution Networks: Clock system architectures, Clock Generation circuits and Clock Distribution Networks. Phase-Locked Loops/Delay-Locked Loops: Charge Pump PLLs, All Digital PLLs and Delay Locked Loops.

Input/Output Modules and ESD Protection Networks: General Chip Organizations: Power Pads and I/O Pads. Input Buffers: Schmitt Circuits, Level-Shifting Circuits and Differential Buffers. Output Drivers / Buffers. Electrostatic Discharge Protection Networks.

Text 1:14.1- 14.3, 15.1- 15.4

Self-Study Component:	3. Perform the power analysis for the given digital circuits.

UNIT – V	**8 Hours**

Design Economics: Nonrecurring Engineering Costs (NREs), Recurring Costs, Fixed Costs, Schedule, Person power, Project Management, Design reuse.

Testing, Verification, and Testable Designs: An Overview of VLSI Testing: Verification testing, Wafer test and Device test. Fault Models: Stuck at faults, Equivalent faults, Bridge and stuck open / stuck closed faults and delay faults, Fault detection. Automatic Test Pattern Generation, Testable Circuit Designs: Ad hoc Approach, Scan-Path Method and Built-in Self-Test and Boundary-Scan Standard—IEEE 1149.1. System-Level Testing: SRAM BIST and March Test.

Text 1: 16.1-16.5.

Text 2: 14.5-14.5.7.

Self-Study Component:	1. Explore the advantages of Multiple Antenna Transmission in LTE 2. Understand the concept of Cell Acquisition Procedure in LTE

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	***Apply*** the knowledge the VLSI System Design Methodology, Chip Design Methods and various concepts of Design Capture Tools.	L3	PO1 [L3]
CO2	***Analyze*** the Data Path Sub System Design and Array Subsystem Design.	L4	PO1 [L4]
CO3	***Develop*** the memory system and Special Purpose Subsystems.	L6	PO1 [L5]
CO4	***Design*** and ***develop*** VLSI System Testing & Verification.	L4,L6	PO1,PO4,PO5 [L4,L6]

Text Book(s):

1. **"**Introduction to VLSI Systems: A Logic, Circuit, and System Perspective**" ,** Ming-Bo Lin, CRC Press, ISBN-10: 143986859X, ISBN-13: 978-1439868591, 2011.
2. **"CMOS VLSI Design: a Circuits and Systems Perspective",** Neil H. E. Weste, David Money Harris, Pearson, 4th edition, ISBN 10: 0-321-54774-8, ISBN 13:978-0-321-54774-3

Reference Book(s):

1. **"Basic VLSI Design**", Douglas A Pucknell and Kamran Eshragian, PHI 3rd Edition, ISBN 13: 9788120309869. (original Edition – 1994).
2. "**Modern VLSI design: System on Silicon" Pearson Education**", Wayne, Wolf,

2nd edition, ISBN: 81-7758-411-1, 1998.

Web and Video link(s):

1. https://youtu.be/AhiQeP002ZU
2. https://youtu.be/otOSL1ZLnOo
3. https://youtu.be/4eabTjqmF-g

E-Books/Resources:

1. https://archive.org/details/cmosvlsidesignacircuitsandsystemsperspective_201908
2. https://www.google.co.in/books/edition/Introduction_to_VLSI_Systems/K0XOBQAAQBAJ?hl=en&gbpv=1&printsec=frontcover

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	2				
#2	2				
#3	2				
#4				2	2

RF Integrated circuits

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – II

Course Code:	**P22MECE254**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- To Understand the behavior of Passive and Active components for RF signals.
- To Analyze the impact of noise and environmental variations on the working of RF circuits.
- To Analyze and design of amplifiers, oscillators and mixers.
- To Evaluate the performance parameter of amplifiers, oscillators and mixers.
- To Understand the transceiver architecture and its related components.

UNIT – I	**8 Hours**

RF Components: Electric Fields and Capacitance, Magnetic Fields and Inductance, Time-Varying Fields and Maxwell Equations, LC and RLC Circuits, Antennas, Integrated Capacitors, Integrated Inductors.

RF Networks: Introduction to Two Ports, Available Power, Impedance Transformation, Lossless Transmission Lines, Receive–Transmit Antennas as Two-Port Circuits, Scattering Parameters, Differential Two-Ports.

Text 1:1.1-1.3,1.7,1.9,1.10,1.11,3.1-3.4,3.6,3.8,3.9.

Self-Study Component:	1. Distributed and Lumped Circuits, Network functions.

UNIT – II	**8 Hours**

RF and IF: Filters: Ideal Filters, Doubly Terminated LC Filters, And Active Filters.

Noise: Two-Port Equivalent Noise, Noise Figure, Impact of Feedback on Noise Figure, Phase Noise, Sensitivity.

Text 1:4.1-4.3,5.2,5.3,5.5,5.7,5.8.

Self-Study Component:	1. Stability of filter and related design parameter. 2. Stability of surface and bulk acoustics wave.

UNIT – III	**8 Hours**

Low-Noise Amplifiers: Matching Requirements, RF Tuned Amplifiers, Common-Source and Common-Gate LNAs, Series Feedback LNAs, LNA Design Case Study

Mixers: Mixers Fundamentals, Evolution of Mixers, Active Mixers, Passive Current-Mode Mixers.

Text 1:7.1-7.5,7.10,8.1-8.4.

Self-Study Component:	1. Impact of feedback topology, biasing, substrate on low noise amplifiers. 2. Second order distortion and its effects on active mixers.

UNIT – IV	**8 Hours**

Oscillators: The Linear LC Oscillator, The Nonlinear LC Oscillator, Phase Noise Analysis of the Nonlinear LC Oscillator, LC Oscillator Topologies, Q-Degradation, Frequency Modulation Effects, More LC Oscillator Topologies, Ring Oscillators, Quadrature Oscillators

Power Amplifiers: Class A Pas, Class B Pas

Text 1:9.1-9.9,11.2,11.3.

Self-Study	1. Design and simulate oscillator and amplifiers for given

Component:	requirements

UNIT – V	**8 Hours**

Transceiver Architectures: General Considerations, Receiver Architectures, Blocker-Tolerant Receivers, Receiver Filtering and ADC Design, Receiver Gain Control, Transmitter Architectures, Transceiver Practical Design Concerns.
Text1:12.1-12.7.

Self-Study Component:	3. Study of Bluetooth Transceiver Architecture.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Apply** fundamentals of field theory,circuit analysis and MOSFET'S to understand the RF blocks and circuits.	L2	PO1[L2]
CO2	**Design** RF circuits for oscillators, power amplifiers and Mixers	L4	PO2[L4]
CO3	**Analyze** the impact of topology and substrate effects of RF circuits.	L3	PO3[L3]
CO4	**Illustrate** the significance and role of RF blocks in communication modules.	L3	PO4[L3] PO5[L3]

Text Book(s):
"Radio Frequency Integrated Circuits and Systems",Second Edition HOOMAN DARABI Broadcom Inc., Irvine

Reference Book(s):
1. RF Microelectronics by Behzad Razavi, Second Edition, Pearson, ISBN 978-0-13-71347
2. The Design Of CMOS Radio-Frequency Integrated Circuits by Thomas H. Lee,Second Edition, Cambridge University Press ISBN 0-521-83539-9
3. VLSI for Wireless Communication by Bosco Leung, Second Edition, Prentice Hall -
4. Electronics and VLSI Series, ISBN 978-1-4614-0985-4

Web and Video link(s):
1. https://nptel.ac.in/courses/117102012
2. https://archive.nptel.ac.in/courses/117/102/117102012/
3. http://www.eleceng.ohio-state.edu/~roblin/durip/OSUresearch/

E-Books/Resources:
3. https://assets.cambridge.org/97811071/94755/frontmatter/9781107194755_frontmatter.pdf

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2		3			
#3			3		
#4				2	1

VLSI and Embedded System Laboratory - II			
Course Code	P22MECEL27	**L-T-P-H :**	1-0-2-3
Contact Period	36 Hrs	**CIE**	50
Exam:	3 Hrs.	**SEE:**	50

Course Content

A. Analog Design

Analog Design Flow:

Design the following circuits with given specifications*, completing the design flow mentioned below:

a. Draw the schematic and verify the following
   DC Analysis, AC Analysis and Transient Analysis
b. Draw the Layout and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design.

1. Basic gates and universal gates
2. A Single Stage differential amplifier
3. Common source and Common Drain amplifier
4. Design an op-amp with given specification* using differential amplifier Common source amplifier in library**
5. Design a 4/8 bit R-2R based DAC for the given specification
6. Design a simple 4/8-bit ADC converter using any one of the tools given above

B. Embedded System

1. Interface and Control of on-board LEDs (signaling) through Switch control (Sensors).
2. Interface and smart control of Motors (application specific).
3. Establishing Wired/Wireless Communication using peripherals.
4. Interfacing different Display or Output peripherals with Processor.
5. Measurement of Time and Frequency using Timers and interrupts.
6. Develop a system to count the number of vehicle passed on road. Get the input from relevant sensor and perform the operation.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Program Outcome Addressed (PO #) with BTL**
CO1	**Apply** the knowledge of the digital system to design of the schematic and layout in cadence tools and apply embedded system principles to interface and control on-board LEDs and motors through sensors and switches	**PO1 (L1), PO2(L2)**
CO2	**Interpret** the outcome of DC Analysis, AC Analysis and Transient Analysis in analog circuits and understand wired and wireless communication protocols and their implementation in embedded systems	**PO4, PO9 (L4)**
CO3	**Design** and **simulate** basic CMOS circuits like inverter,common source amplifier and differential amplifiers and and analyze different techniques for interfacing display and output peripherals with processors for specific applications in embedded systems.	**PO3, PO5, PO8, (L5)**
CO4	**Analysis** of the **design** for DRC, LVS and QRC of the analog circuits and also develop Time and Frequency Measurement Systems	**PO2, PO5 (L4)**

	in embedded systems.	
CO5	Implement DAC and ADC Designs in cadence and Develop Vehicle Counting Systems in embedded application.	**PO3, PO5, PO7, (L5)**

Text Book(s):

1. **"The Definitive Guide to ARM_ Cortex_-M3 and Cortex-M4 Processors"**, Joseph Yiu,3rd edition , Newness publications, ISBN 13: 978-0-12-408082-9, 2016**.**
2. **"Design of Analog CMOS Integrated Circuits",** Behzad Razavi, 2nd edition Tata McGraw Hill, ISBN 978-0-07-252493-2 2017.

Course Articulation Matrix (CAM)

CO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2
#1	3	2			2				2				3	
#2		2	2	2	2				3					
#3			2		3			2						
#4		3			3									3
#5			2		3		2							

Semester-III

Multicore Architecture and Programming
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – III

Course Code:	**P22MECE31**	**Credits:**	**04**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to

- Understand the concept of multi–core architecture and system overview of threading.
- Cover fundamental concepts of parallel programming and its constructs.
- Describe in detail the concepts of threading APIs.
- Explain the different aspects of OpenMP.
- Use OpenMP for parallel programming

UNIT – I	**8 Hours**

Introduction to Multi– core Architecture: Motivation for Concurrency in software, Parallel Computing Platforms, Parallel Computing in Microprocessors, Differentiating Multi–core Architectures from Hyper– Threading Technology, Multithreading on Single–Core versus Multi–Core Platforms Understanding Performance, Amdahl's Law, Growing Returns: Gustafson's Law. System Overview of Threading: Defining Threads, System View of Threads, Threading above the Operating System, Threads inside the OS, Threads inside the Hardware, What Happens When a Thread Is Created, Application Programming Models and Threading.

Text 1: Chapters 1 and 2

Self-Study Component:	**1.** Undersand the concepts present in the thesis: Bulpin, James Roy. 2004. Operating System Support for Simultaneous Multithreaded Processors. PhD thesis, King's College, University of Cambridge, September.

UNIT – II	**8 Hours**

Fundamental Concepts of Parallel Programming: Designing for Threads, Task Decomposition, Data Decomposition, Data Flow Decomposition, Implications of Different Decompositions, and Challenges You will Face, Parallel Programming Patterns. A Motivating Problem: Error Diffusion, Analysis of the Error Diffusion Algorithm. An Alternate Approach: Parallel Error Diffusion, Other Alternatives. Threading and Parallel Programming Constructs: Synchronization, Critical Sections,
Deadlock, Synchronization Primitives, Semaphores, Locks, Condition Variables, Messages, Flow Control–based Concepts, Fence, Barrier

Text 1: Chapters 3 and 4

Self-Study Component:	**1.** Study and write a report on: Barney, Blaise. Introduction to Parallel Computing. Lawrence Livermore National Laboratory, Livermore Computing.Available at: http://www.llnl.gov/computing/tutorials/parallel_comp/.

UNIT – III	**8 Hours**

Solutions to Common Parallel Programming Problems: Too Many Threads, Data Races, Deadlocks, and Live Locks, Deadlock, Heavily Contended Locks, Priority Inversion, Solutions for Heavily Contended Locks, Non–blocking Algorithms, ABA Problem, Cache Line Ping– ponging, Memory Reclamation Problem, Recommendations, Memory Issues, Bandwidth, Working in the Cache, Cache related Issues, False Sharing, Memory Consistency.

Text 1: Chapter 7	
Self-Study Component:	**1.** Study and write a report on: Blumofe, Robert D., Christopher F. Joerg, Bradley C. Kuszmaul, Charles E. Leiserson, Keith H. Randall, and Yuli Zhou. 1995. Cilk: An Efficient Multithreaded Runtime System. Proceedings of the 5th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (July):207–216.

UNIT – IV	**8 Hours**

OpenMP: A Portable Solution for Threading Challenges in Threading a Loop, Loop–carried Dependence, Data– race Conditions, Managing Shared and Private Data, Loop Scheduling and Portioning, Effective Use of Reductions, Minimizing Threading Overhead, Work–sharing Sections, Performance– oriented Programming, Using Barrier and No wait, Interleaving Single– thread and Multi– thread Execution, Data Copy–in and Copy–out, Protecting Updates of Shared Variables, OpenMP Library Functions, OpenMP Environment Variables, Compilation, Debugging, performance.

Text 1: Chapter 6

Self-Study Component:	**1.** Understand the concepts: Hill, Mark D. 1998. Multiprocessors Should Support Simple Memory Consistency Models. IEEE Computer (August), 31(8):28–34.

UNIT – V	**8 Hours**

OpenMP Language Features: Introduction Terminology Parallel Construct Sharing the Work among Threads in an OpenMP Program Clauses to Control Parallel and Work-Sharing Constructs OpenMP Synchronization Constructs Interaction with the Execution Environment More OpenMP Clauses Advanced OpenMP Constructs .

Text 2: Chapter 4

Self-Study Component:	**1.** Understand multithreaded programming: Mattson, Tim. Nuts and Bolts of Multithreaded Programming. Santa Clara, CA: Intel Corporation. Available at: http://www.intel.com.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Evaluate** the Multicore Hardware and Software concepts.	L1	PO1 (L1)
CO2	**Analyze** the Parallel Programming concepts with examples along with Deadlocks and Semaphores.	L3	PO1 (L3)
CO3	**Develop** the theories related to parallel programming problems and methods to overcome them.	L3	PO1 (L2), PO2 (L3)
CO4	**Describe** the various programming concepts of OpenMP with examples.	L3	PO3 (L3)

Text Book(s):

1. Multicore Programming, Increased Performance Through Software Multi–threading, Shameem Akhter and Jason Roberts, Intel Press, 2006. ISBN 0-9764832-4-6.
2. Using OpenMP, Portable Shared Memory Parallel Programming, Barbara Chapman, Gabriele Jost, Ruud van der Pas, 2008, ISBN 978-0-262-53302 MIT Press, Massachusetts Institute of Technology

Reference Book(s):

1. Principles of Parallel Programming, Calvin Lin, Lawrence Snyder, Pearson Education, 2009. ISBN-13: 978-0321487902.
2. Parallel Programming in C with MPI and OpenMP, Michael J. Quinn, Tata McGraw Hill, 2004. ISBN 13: 9780070582019.
3. Parallel Computer Architecture A Hardware / Software Approach David E, Culler, Jaswinder Pal Singh with Anoop Gupta, ISBN: 9781558603431.

Web and Video link(s):

1. Multi-Core Computer Architecture – Storage and Interconnects, NPTEL IIT Guwahati. https://www.youtube.com/playlist?list=PLwdnzlV3ogoU0TR333JyxG8T3HDg52S0h
2. Introduction to parallel Programming in Open MP https://www.youtube.com/playlist?list=PLJ5C_6qdAvBFMAko9JTyDJDIt1W48Sxm

E-Books/Resources:

1. Introduction to Computer Systems https://www.cs.cmu.edu/~fp/courses/15213-s07//schedule.html

Course Articulation Matrix (CAM)

CO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO2
#1	1												1	
#2	3												3	
#3	2	3											2	3
#4			3											

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Professional Elective –V

HIGH-PERFORMANCE DIGITAL VLSI CIRCUIT DESIGN
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – III

Course Code:	**P22MECE321**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- To Understand the operational aspects of devices, families and circuits.
- To analyze the circuits propagation delay and power dissipation.
- To evaluate the models, topologies and circuits for performance parameters.
- To design modular blocks for the given specifications.

UNIT – I	**8 Hours**

Electronics Fundamentals: Comparisons Between Bipolar and MOS Transistors, CMOS Digital Circuits, Bipolar ECL Circuits, BiCMOS Circuits, Power-Delay Tradeoffs Between CMOS, Bipolar ECL and BiCMOS Circuits.
Device Design Considerations: Design Considerations for Bipolar Transistors, Cutoff Frequency, BiCMOS Device Design Considerations, BiCMOS Device Scaling.
CMOS High-Performance Circuits: Static Digital CMOS Circuits, Non-Pipelined Dynamic CMOS Circuits.
Text 1: 1.1-1.5, 2.2-2.5,4.1,4.2.

Self-Study Component:	2. Study the Modeling of the MOS Transistor. 3. Study the Modeling of the Bipolar Transistor.

UNIT – II	**8 Hours**

CMOS High-Performance Circuits: Pipelined Dynamic CMOS Circuits, An All-N-Logic Single-Phase Pipelined Dynamic CMOS Logic, Circuit Structures and Operational Principles, Circuit Optimization and Evaluation, Circuit Examples.
Text 1: 4.3, 4.4.1,4.4.2,4.4.3.
A CML Propagation Delay Model: CML and ECL Previous Delay Models, New CML Propagation Delay Model, Transient Analysis, High-Current Effects, Model Verification and Its Application in Circuit Optimization, Model Limitations.

Text 2: 5.2-5.7.

Self-Study Component:	4. Study of CMOS Circuits. 5. Analyze various Delay model.

UNIT – III	**8 Hours**

Series-Gated CML and ECL Bipolar Circuits: Two-level Series-gating CML and ECL Circuit Design, Analysis and Optimization of Two-level Circuits.
Text 1: 6.2, 6.3.
High-Performance BiCMOS Circuit Structures: ECL/CMOS Interface Circuits, Dynamic ECL Reference Voltage (DRV) CMOS/ECL Interface Circuits.
Text 2: 7.2,7.3.

Self-Study Component:	4. Explore on Bipolar circuits. 5. Illustration on BiCMOS circuit.

UNIT – IV	**8 Hours**

High-Performance BiCMOS Circuit Structures: BiCMOS Sense Amplifiers for SRAM.

Text 1: 7.4
High-Performance CML, ECL and NTL BICMOS Circuits: Low-Power Circuits and Systems, BJT and MOS Series-Gated CML Circuit Techniques, Performance of XOR, D-Iatch BJT and MOS Series-Gated Circuits, Performance of CML D-Latch Comparator Circuits, High-Performance ECL Circuit Techniques, Active Load (Series Diode and Resistor), Active-Pull-Down Techniques, Discussion and Assessment of Active-Pull-Down ECL Circuit Techniques, BiCMOS Active-Pull-Down ECL Circuit Technique, Non-Threshold-Logic Circuits, Conventional NTL Circuits, APD-NTL Circuit Techniques.
Text 2: : 8.2- 8.13.

Self-Study Component:	2. Study of low-power circuits. 3. Explore on various circuit technique.

UNIT – V	**8 Hours**

High-Performance CML, ECL and NTL BICMOS Circuits: APD-NTL Circuit Performance, Applications.
High-Performance System Applications: Phase-Locked Loops, Phase-Locked Loop Building Blocks.
Text 1: 8.14,8.15,9.9-9.3.

Self-Study Component:	4. Study of BICMOS circuits applications. 5. Explore on various system applications.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Apply** the fundamentals of MOSFETs to understand performance aspects of logic families and their structures.	L2	PO1[L2]
CO2	**Characterize** the logic family structure and their delay performance.	L3	PO4 [L3]
CO3	**Design** a logic structure for given application requirements.	L4	PO3 [L4]
CO4	**Interpret** the working and significance of logic blocks in High Performance integrated circuits.	L3	PO1, PO3 [L3]

Text Book(s):
"HIGH-PERFORMANCE DIGITAL VLSI CIRCUIT DESIGN", Richard X. Gu ,University of Waterloo, Khaled M. Sharaf, University of Waterloo Mohamed I Elmasry, ISBN 978-1-4613-5970-8 ISBN 978-1-4615-2297-3 (eBook), DOI 10.1007/978-1-4615-2297-3.

Reference Book(s):
"**DIGITAL BiCMOS INTEGRATED CIRCUIT DESIGN",** Springer Science+ BusÎness Media, LLC Library of Congress Cataloglng-ln-Publlcatlon Data Embabi, S. H. K. (Sherif H. K.), ISBN 978-1-4613-6391-0 ISBN 978-1-4615-3174-6 (eBook), DOI 10.1007/978-1-4615-3174-6.

Web and Video link(s):
1. https://www.tsmc.com/static/english/campaign/VLSI2020/index.htm
https://semiwiki.com/semiconductor-manufacturers/intel/314047-intel-4-presented-at-vlsi/
2. https://www.youtube.com/watch?v=WDo58OseTJw.

E-Books/Resources:

4. https://link.springer.com/book/10.1007/978-1-4615-2297-3
5. https://www.amazon.in/High-Performance-Springer-International-Engineering-Computer/dp/1461359708

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2				3	
#3			2		
#4	3		2		

NETWORK ON CHIP

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – III

Course Code:	**P22MECE322**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- To understand the different routing algorithms.
- To analyze different architecture design.
- To design different mapping techniques.
- To understand Fault Controlling Techniques.
- To design NoC topologies.

UNIT – I **8 Hours**

Introduction: System-on-Chip Integration and Its Challenges, SoC to Network-on-Chip: A Paradigm Shift, Research Issues in NoC Development, Existing NoC Examples.

Interconnection Networks in Networks-on-chip: Introduction, Network Topologies, Switching Techniques, Routing Strategies, Flow Control Protocol, Quality-of-Service Support, NI Module.

Text 1:1- 1.1, 1.2, 1.3, 1.4, 2- 2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7.

Self-Study Component:	Study on Benefits and Challenges of Adopting NoCs.

UNIT – II **8 Hours**

Architecture Design of Network-on-Chip: Introduction, Switching Techniques and Packet Format, Asynchronous FIFO Design, GALS Style of Communication, Wormhole Router Architecture Design, VC Router Architecture Design, Adaptive Router Architecture Design.

Text 1: 3 – 3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7.

Evaluation of Network-on-chip Architectures: Evaluation Methodologies of NoC, Traffic Modeling, Selection of Channel Width and Flit Size, Simulation Results and Analysis of MoT,

Performance and Cost Comparison of MoT with other NoC Structures having VC Router, Limitations of Tree- Based Topologies.

Text 1: 4 – 4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9.

Self-Study Component:	Case study on Power and Thermal Effects and Management.

UNIT – III **8 Hours**

Application Mapping on Network-on-chip: Introduction, Mapping problem, ILP Formulation,

Constructive Heuristics for Application Mapping, Constructive Heuristics with Iterative Improvement, Mapping using Discrete PSO.

Text 1:5 – 5.1, 5.2, 5.3, 5.4, 5.5, 5,6.

Low-Power Techniques for Network-on-chip: Introduction, Standard Low-Power Methods for NoC Routers, Standard Low-Power Methods for NoC Links, System-level Power Reduction.

Text 1:6 – 6.1, 6.2, 6.3, 6.4.

Self-Study Component:	Develop a NoC Architecture in SytemC.

UNIT – IV **8 Hours**

Signal Integrity and Reliability of Network-on-chip: Introduction, Sources of Faults in NoC Fabric, Permanent Fault Controlling Techniques, Transient Fault Controlling

Techniques, Unified Coding Framework, Energy and Reliability Trade-off in Coding Technique.
Text 1:7 – 7.1, 7.2, 7.3, 7.4 7.5 7.6.
Testing of Network-on-Chip Architectures: Introduction, Testing Communication Fabric, Testing Cores.
Text 1: 8 – 8.1, 8.2, 8.3.

Self-Study Component:	Study on Spidergon STNoC.

UNIT – V	**8 Hours**

Application-Specific Network-on-chip Synthesis: Introduction, ASNoC Synthesis Problem, Literature Survey, System-Levels Floor planning, Custom Interconnection Topology and Route Generation, ASNoC Synthesis with Flexible Router Placement, PSO for Flexible Router Placement, PSO for Flexible Router Placement.
Text 1: 9 – 9.1, 9.2, 9.3, 9.4, 9.5,9.6.
Reconfigurable Network-on-chip Design: Introduction, Literature Review, Local Reconfiguration Approach, Topology Reconfiguration, Link Reconfiguration.
Chapter 10 – Introduction, Literature Review, Local Reconfiguration approach, Topology Reconfiguration, Link Reconfiguration.
Text 1: Chapter 10 – 10.1, 10.2, 10.3, 10.4, 10.5.

Self-Study Component:	Case study on Middleware Memory Management in NoC.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Identify** and **Describe** network topologies, Noc architecture and low power routing methods	L2	PO1
CO2	**Compare** Noc architecture, network topologies and low power techniques	L4	PO2
CO3	**Investigate** the network on chip for signal integrity and reliability.	L5	PO2
CO4	**Outline** floor planning and synthesis mechanisms with Noc reconfigurability.	L1	PO1

Text Book(s):
Santanu Kundu, Santanu Chattopadhyay**" Network-on-Chip: The Next Generation of System on-Chip Integration"**,2014 CRC Press

Reference Book(s):
1. ChrysostomosNicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-on - Chip Architectures Holistic Design Exploration", Springer. Fayezgebali, Haythamelmiligi, Hqhahed Watheq E1-Kharashi "Networks-on-Chips theory and practice CRC press.
2. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-on-Chip Architectures" 2013. ISBN : 978-1-4614-4273-8
3. Palesi, Maurizio, Danesh talab, Masoud "Routing Algorithms in Networks-on-Chip" 2014

Web and Video link(s):
1. https://youtu.be/7-KJ3BnFsr8
2. https://youtu.be/zSapXphjQzY

E-Books/Resources:

1. ISBN 978-1-4614-4274-5 (eBook)
2. 978-1-4398-3711-5 (Ebook-PDF)

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2		3			
#3		2			
#4	2				

Real Time Operating Systems

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – III

Course Code:	P22MECE323	**Credits:**	03
Teaching Hours/Week (L:T:P):	3:0:0	**CIE Marks:**	50
Total Number of Teaching Hours:	40	**SEE Marks:**	50

Course Learning Objectives (CLOs)

This course will enable the students to:

1. Understand the basic concept of real time embedded system.
2. Explain the concepts of scheduling in RTOS.
3. Describe the concepts of Processing, I/O Resources, Memory.
4. Explain the concept of Multi-resource Services.
5. Explain the differences between hard-time and Soft Real-Time Services.
6. Understand the basic concepts of Embedded System Components and Debugging Components.
7. Illustrate the concept Performance Tuning.
8. Design the RTOS and Reliability.

UNIT – I	**8 Hours**

Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems.

System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS,

Text 1: 1.1,1.2,1.3, 2.1-2.8.

Self-Learning Component:	Thread Safe Reentrant Functions.

UNIT – II	**8 Hours**

Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Montonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies.

I/O Resources: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.

Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, systems.

Text 1: 3.1-3.7,4.1-4.5,5.1-5.5

Self-Learning Component:	Flash file

UNIT – III	**8 Hours**

Multi-resource Services:

Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.

Soft Real-Time Services:

Missed Deadlines, QoS, Alternative to rate monotonic policy.

Text 1: 6.1-6.5,7.1-7.5

Self-Learning Component:	Mixed hard and soft real-time services

UNIT – IV	**8 Hours**

Embedded System Components:

Firmware components, RTOS system software mechanisms, Software application components.

Debugging Components:
Exceptions, assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self-test and diagnostics, External test equipment, Application-level debugging.
Text 1: 8.3,8.4,8.5,12.1-12.11

Self-Learning Component:	Application-level debugging.

UNIT – V	**8 Hours**

Performance Tuning:
Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency, and Call frequency, Fundamental optimizations.
High availability and Reliability Design:
Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design tradeoffs, Hierarchical applications for Fail-safe design.
Design of RTOS – PIC microcontroller.
Text 1: 13.1-13.6, 14.1-14.6

Self-Learning Component:	Fundamental optimizations

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	Apply the knowledge the I/O resources to understand the execution time, deadline and architecture and memory.	Apply	PO1[L1]
CO2	Analyze the concepts of scheduling in RTOS.	Analyze	PO2[L2]
CO3	Design debugging componentswhile understanding the concept of critical section of shared resources.	Create	PO3[L3]
CO4	Evaluate the quality of services of soft real time operating system.	Evaluate	PO3[L4]

Text Book(s):

1. **"Real-Time Embedded Systems and Components",**SamSiewert, Cengage Learning India Edition, 2007.

Reference Book(s):

1. **"Programming and Customizing the PIC Microcontroller",** MykePredko, 3rd Edition, TMH, 2008.
2. **"Programming for Embedded Systems**", Dreamtech Software Team, John Wiley, India Pvt. Ltd., 2008

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5
#1	**3**				
#2		**3**			
#3			**3**		
#4			**3**		

VLSI Testing and Verification			
Course Code:	P22MECE324	**Credits:**	03
Teaching Hours/Week (L:T:P):	3 : 0 : 0	**CIE Marks:**	50
Total Number of Teaching Hours:	40	**SEE Marks:**	50

Course Learning Objectives (CLOs)

This course will enable the students to:

1. Provide the basic knowledge of VLSI Testing and Verification.
2. Provide the understanding of Test Generation for Combinational Logic Circuits.
3. Design a Testable Combinational Logic Circuits and Sequential Circuits.
4. Explain the concept of Verification Tools and Verification languages.
5. Outline the concepts of waveform generation and test benches.

UNIT – I	8 Hours

Faults in Digital Circuits: Failures and Faults, Modeling of Faults: Stuck at Faults, Bridging Faults, Breaks and transistor Stuck –On/Open Faults in CMOS.

Test Generation for Combinational Logic Circuits: Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits.

Text 1:1.1, 1.2, 2.1, 2.2.1, 2.2.2, 2.2.3, 2.2.4.

Self-Learning Component:	Temporary Faults, FAN, Delay Fault detection.

UNIT – II	8 Hours

Testable Combinational Logic Circuit Design: The Reed-Muller Expansion Technique, Three-Level OR-AND-OR Design, Automatic Synthesis of Testable Logic, Synthesis of Random Pattern Testable Combinational Circuits, Testable PLA Design.

Test Generation for Sequential Circuits: Testing of Sequential Circuits as Iterative Combinational Circuits, State Table Verification, Test Generation Based on Circuit Structure,

Text1:3.1,3.2,3.3,3.5,3.7,4.1,4.2, 4.3.

Self-Learning Component:	Testable design of Multilevel Combinational circuits, Path delay faults testable combinational Logic Design, Functional Fault Models.

UNIT – III	8 Hours

Design of Testable Sequential Circuits: Controllability and Observability, Ad Hoc Design Rules for Improving Testability, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design.

Built-In Self-Test: Test Pattern Generation for BIST, Output Response Analysis, BIST Architectures.

Text 1: 5.1, 5.2, 5.4, 5.5, 6.1, 6.2, 6.4.

Self-Learning Component:	Design of Diagnosable Sequential Circuits, Random Access Scan Technique, Cross Talk, Circular BIST.

UNIT – IV	8 Hours

What is verification: What is testbench, Importance of verification, Reconvergence model, Human factor, What is being verified.

Verification Tools: Linting tools, Simulators, Waveform viewers, Code coverage, Verification languages, Issue Tracking.

Text 2: Chapter-1, Chapter-2.

Self-Learning Component:	Functional verification approaches, Third party models, Revision Control.

UNIT – V	8 Hours
Stimulus and Response: Simple Stimulus: Generating a simple waveform, Generating a Complex waveform, Generating Synchronised Waveforms, Aligning Waveforms in Delta-Time, Generating Synchronous Data Waveforms, Encapsulating Waveform Generation, Abstracting Waveform Generation, Verifying the output: Visual Inspection of Response,Producing Simulation Results, Minimizing Sampling, Visual Inspection of Waveforms. Self checkingTestbenches: Input and Output Vectors, Golden Vectors, Run-Time Result Verification.	
Self-Learning Component:	Predicting the output: Data Formatters, Packet Processors, Complex Transformations.

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	**Apply** the knowledge of Digital and Analog VLSI circuits to understand the concepts of VLSI Circuit testing.	Apply	PO1 (L2)
CO2	**Analyze** the various concepts of test generation for combinational, sequential logic circuits and BIST.	Analyze	PO2 (L2)
CO3	**Design** the testable combinational, sequential logic circuits and BIST for the given specifications.	Create	PO3 (L3)
CO4	**Analyze** the Verification tools, Verification languages. and Stimulus and Response in verification	Analyze	PO2 (L2)

Text Book(s):

1. **"Digital Circuit Testing and Testability"**, Parag. K. Lala, Academic Press, ISBN 0-12-434330-9.
2. **"Writing Test Benches: Functional Verification of HDL Models"**, JanickBergeron,2nd edition Kluwer Academic Publishers,2003, ISBN 1-4020-7401-8.

Reference Book(s):

1. **"Digital Systems and Testable Design"**, M. Abramovici, M.A. Breuer and A.D. Friedman, Jaico Publishing House, 2002, ISBN 0-7803-1062-4.
2. **"Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits"**, M.L. Bushnell and V.D. Agrawal, Kluwar Academic Publishers, ISBN 978-0-306-470470-0.

Web and Video link(s):

1. VLSI Testing (http://www.ee.ncu.edu.tw/~jfli/vlsi21/lecture/ch06.pdf)
2. NPTEL Course on Design Verification and test of Digital VLSI circuits, by DrSanthoshBiswas and DrJitendra Kumar Deka, IIT Guhathi, https://nptel.ac.in/courses/106/103/106103116/

E-Books/Resources:

1. https://www.gettextbooks.com/isbn/9780124343306/
2. https://vlsitesting.files.wordpress.com/2017/02/ref-for-unit5.pdf

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	2				
#2		2			
#3			2		
#4		2			

Open Elective

EMBEDDED SYSTEMS
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – III

Course Code:	**P22MECEO331**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Provide the knowledge about basic concepts of Embedded Systems.
- Outline the concepts of typical embedded systems communication buses.
- Provide the knowledge of software hardware co–design and basic programming concepts.
- Describe the concepts of real time operating system based embedded systems.
- Describe some embedded system representative models along with recent trends.

UNIT – I	**8 Hours**

Introduction to Embedded Systems: Embedded systems, Processor Embedded into a System, Embedded Hardware Units and Devices in a System, Embedded Software in a System, Examples of Embedded Systems, Embedded System-on-chip (Soc) and Use of VLSI Circuit Design Technology, Complex System Design and Processors, Design Process in Embedded System, Formalization of System Design, Design Process and Design Examples, Classification of Embedded Systems, Skills Required for an Embedded System Designer.
Text 1: 1.1-1.12

Self-Study Component:	1. Analyze the different Characteristics and Quality Attributes of Embedded Systems.

UNIT – II	**8 Hours**

Devices and Communication Buses for Devices Networks: IO Types and Examples, Serial Communication Devices, Parallel Device Ports, Sophisticated Interfacing Features in Device Ports, Wireless Devices, Timer and Counting Devices, Watchdog Timer, Real Time Clock, Network Embedded Systems, Serial Bus Communication Protocols, Parallel Bus Device Protocols-Parallel Communication Network Using ISA,PCI,PCI-X and Advanced Buses, Internet Embedded Systems-Network Protocols, Wireless and Mobile System Protocols.
Text 1: 3.1-3.13

Self-Study Component:	1. Study other system components required to design embedded systems. 2. Study the working of Hydraulic and Rotatory Actuators to understand the Operation of output devices.

UNIT – III	**8 Hours**

Programming Concepts and Embedded Programming in C,C++ and JAVA: Software Programming in Assembly Language(ALP) and in High Level Language 'C',C Program Elements: Header and Source Files and Processor Directives, Object-Oriented Programming, Embedded Programming in C++, Embedded Programming in Java.
Program Modeling Concepts: Program Models, DFG models, State Machine Programming Model for Event-controlled Program Flow, Modeling of Multiprocessor Systems, UML Modeling.
Text 1:5.1-5.2, 5.5-5.7, 6.1-6.5

Self-Study Component:	1. Create a state diagram that shows how UML usage for designing a door system (that can only be opened and closed).

	2. Discuss the different languages used in embedded system design and implement any one particular embedded application.
UNIT – IV	**8 Hours**
Embedded/Real-Time Operating System Concepts: Architecture of the Kernel, Task and Task Scheduler, Interrupt Service Routines, Semaphores, Mutex, Mailboxes, Message Queues, Event Registers, Pipes, Signals, Timers, Memory Management, Priority Inversion Problem. **Overview Of embedded/Real –Time Operating Systems:** Off –the –Shelf Operating Systems, Embedded Operating Systems, Real –Time Operating Systems, Handheld Operating Systems. **Text 2: 7.1-7.13, 8.1-8.4**	
Self-Study Component:	1. Understand the basic of Real time operating system using the below link https://youtu.be/dHsHP9RrXBw and present a report on the same.
UNIT – V	**8 Hours**
Embedded Software Development Process and Tools: Introduction to Embedded Software Development Process and Tools, Host and Target Machines, Linking and Locating Software, Getting Embedded Software into the Target System, Issues in Hardware –Software Design and Co-design. **Representative Embedded Systems**: Digital Thermometer, Handheld Computer, Navigation System, IP Phone, Software-defined Radio, Smart Cards, RF Tags. **Future Trends:** Emerging Technologies, Emerging Applications. **Text 1: 13.1-13.5 and Text 2: 10.1-10.7, 22.1-22.2**	
Self-Study Component:	1. Understand and present the concept of Embedded system software by referring the below paper: B. M. Medvedev, S. A. Molodyakov, S. M. Ustinov and S. A. Fyodorov, "**Embedded systems software: Trends in industry and education**",2018 International Symposium on Consumer Technologies (ISCT), 2018,pp. 66-69, doi: 10.1109/ISCE.2018.8408921. 2. Understand and present the concept of software for Embedded Systems using the below link https://youtu.be/IY4xrpJQwOY

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	**Apply** the basic knowledge of Microcontroller to describe the concepts of Embedded/Real Time System design.	L2	PO1[L2]
CO2	Illustrate and Analyze different communication network protocols and programming models for Embedded System Design	L5	PO4[L5]
CO3	**Analyze** and **interpret** embedded software development process involved in designing respective Embedded System according to emerging technology.	L4	PO3[L3] & PO5[L4]
CO4	**Design** and **Develop** domain specific Embedded System and Embedded Real Time Applications.	L3,L5	PO4[L3] & PO5[L5]

Text Book(s):

1. Raj Kamal**, "Embedded Systems: Architecture, Programming and Design",** 3rd Edition 2017, McGraw Hill Education Publisher, ISBN (10)-9789332901490, ISBN(13)-978-9332901490.
2. Dr. K.V.K.K Prasad**, "Embedded/Real-Time Systems: Concepts, Design & Programming",** New Edition 2003, Dreamtech Press Publisher, ISBN(10)-8177224611, ISBN(13)-978-8177224610.

Reference Book(s):

Shibu K V**, "Introduction to Embedded Systems"**, Tata McGraw Hill Education Private Limited, 2009, ISBN (13): 978-0-07-014589-4.

Web and Video link(s):

1. https://nptel.ac.in/courses/108102045
2. https://nptel.ac.in/courses/106105193

E-Books/Resources:

1. https://media.oiipdf.com/pdf/6dcf2173-d68a-4b39-8b7e-110374c53bd9.pdf
2. https://archive.org/details/K.ShibuIntroductionToEmbeddedSystemsTmh2009/page/n57/mode/2u

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	3				
#2				2	
#3			2		1
#4				2	1

MICROCONTROLLER

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – III

Course Code:	**P22MECEO332**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Provide the basic knowledge of embedded systems.
- Outline the architecture of MSP430.
- Usage of instruction sets and addressing modes for writing programs.
- Understand the working and applications of interrupts.
- Utilize the Low-Power Modes for the Operation of MSP430
- Summarize the operation and utilization of timers.

UNIT – I	**8 Hours**

Embedded Electronic Systems and Microcontrollers: What and where are embedded systems, Approaches to Embedded Systems, Small Microcontrollers, Anatomy of a Typical Small Microcontroller, Memory, and Software.

The Texas Instruments MSP430: The Outside View—Pin-Out, the Inside View—Functional Block Diagram, Memory, Memory Mapped input and output, Clock Generator, Exceptions: Interrupts and Resets.

Text 1:1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 2.1, 2.2, 2.3, 2.5, 2.6, 2.7

Self-Study Component:	1. Study and understand the application of MSP430 in real time applications. 2. Understand the environmental development to develop programs for microcontroller.

UNIT – II	**8 Hours**

Architecture of the MSP430 Processor: Central Processing Unit, Addressing Modes, Constant Generator and Emulated Instructions, Instruction set, Examples, Reflections on the CPU and Instruction Set, Resets, Clock system.

Text 1:5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7, 5.8.

Self-Study Component:	1. Light LED's in C and Assembly Language. 2. Access to the microcontroller for programming and debugging along with demonstration boards.

UNIT – III	**8 Hours**

Functions, Interrupts and Low-Power Modes: Functions and Subroutines, What happens when a Subroutine is called?, Storage for Local Variables, Passing Parameters to a Subroutine and Returning a Result, Interrupts, what happens when an interrupt is requested?, Interrupt Service Routines, Issues Associated with Interrupts, Low-Power Modes of Operation.

Text 1: 6.1, 6.2, 6.3, 6.4, 6.6, 6.7, 6.8, 6.9, 6.10.

Self-Study Component:	1. Study of assembly language/ c-programming tools with programming exercises. 2. Develop and Implement a assembly level program to Flash LED's with frequency of 1Hz using software delay and subroutine.

UNIT – IV	8 Hours
Timers: Watchdog Timer, BasicTimer1, Timer_A, Measurement in the Capture Mode, Measurement of time: Press and Release of button, Output in the Continuous Mode, operation of Timer_A in the sampling mode, Timer_B, what Timer where? **Text 1:**8.1, 8.2, 8.3, 8.4, 8.4.1, 8.5, 8.8, 8.9, 8.10.	
Self-Study Component:	1. Study of output in the up mode- Edge-Aligned PWM. 2. Design and develop a assembly level program to generate pseudorandom stream of bits using shift register.
UNIT – V	**8 Hours**
Mixed Signal System: Analog Input and Output: Comparator_A, Analog-to-Digital Conversion: General Issues, Analog-to-Digital Conversion: Successive Approximation, Operation of a switched capacitor SAR ADC. TheADC10 Successive-Approximation ADC, Basic Operation of the ADC10, ADC conversion Sigma-Delta. **Text 1:**9.1, 9.2, 9.3, 9.3.1, 9.4, 9.5, 9.8.	
Self-Study Component:	1. Study of ADC12 Successive-Approximation ADC. 2. Examine whether direct connection to a MSP430 is sufficient or further connection of the signal is required for conversions of analog signals to digital signals

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	***Illustrate*** an overview of the Embedded System and MSP430 Microcontroller.	L2	PO1[L2]
CO2	***Analyze*** the architecture of MSP430 and the programs using various instruction sets of MSP430	L3	PO3[L3]
CO3	***Interpret*** the use of Interrupts and ***Analyze*** subroutines of MSP430.	L2, L4	PO1[L2] &PO5[L4]
CO4	***Analyze*** built in Timers and Counters associated with MSP40 MC	L3	PO2[L3]
CO5	***Analyze*** and describe the Architecture of different Comparator, ADC used in MSP430	L4	PO4[L4]

Text Book(s):

"MSP430 Microcontrollers Basics", John H. Davies, Newnes (Elsevier Science), 2008, ISBN: 978-0-7506-8276-3

Reference Book(s):

1. "Getting Started with the MSP430 Launchpad", Adrian Fernandez, Dung Dang,Newnes (Elsevier Science), 2013, ISBN: 978-0-124116009
2. **"Programmable Microcontrollers with Applications: MSP430 LaunchPad with CCS and Grace"** CemUnsalan, H. DenizGurhan, McGraw Hill Publictions, 2013, ISBN: 978-0071830034.

Web and Video link(s):
https://www.youtube.com/watch?v=l6M7aqN6dmo

E-Books/Resources:

1. https://www.academia.edu/38330666/MSP430_Microcontroller_Basics_John_H_Davies					
Course Articulation Matrix (CAM)					
CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**
#1	**3**				
#2			**3**		
#3	**2**				**3**
#4		**3**			
#5				**3**	

AUTOMOTIVE ELECTRONICS

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – III

Course Code:	**P22MECEO333**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Understand the concepts of Automotive Electronics and its evolution and trends.
- Illustrate the various application of electronics systems and ECU in automotive.
- Describe principles and applications of sensors and actuators in automotive electronics systems.
- Analyze various control systems and communication protocols in automotive.
- Summarize the modern advanced technologies and trends in automotive.

UNIT – I	**8 Hours**

Electronics Fundamentals: Semiconductor Devices, Diodes, Rectifier Circuit, Transistors, Integrated Circuits, Digital Circuits, Binary Number System, Logic Circuits (Combinatorial), Logic Circuits with Memory (Sequential). Timer circuit, Digital Integrated Circuits.
Text 1: Chapter 2.

Self-Study Component:	1. Compare and contrast different automotive systems and components, analyzing their strengths, weaknesses, and applications in various vehicle types and scenarios.

UNIT – II	**8 Hours**

Basic Fundamental: Electrical and electronic systems in the vehicle.

Basic Principles of Networking: Network topology, Network organization.

Automotive Networking: Cross-system functions, Requirements for bus systems, Classification of bus systems, Applications in the vehicle.

The Basic of Electronic Engine control: Motivation for Electronic Engine Control, Exhaust Emissions, Concept of an Electronic Engine control system, Definition of Engine performance terms, Electronic Fuel control system, Idle Speed Control, Electronic Ignition.
Text 1: Chapter 4, and **Text 2.**

Self-Study Component:	1. Analyze a simple electronic engine control system, using concept of basic components and principles. 2. Compare and contrast different types of electronic ignition systems, analyzing their advantages, disadvantages, and applications in various engines and scenarios.

UNIT – III	**8 Hours**

Automotive Sensor: Airflow rate sensor, Engine Crankshaft Angular Position Sensor, Magnetic Reluctance Position Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle Angle Sensor (TAS), Engine Coolant Temperature (ECT) Sensor, Knock Sensor.
Text 1: Chapter 5.

Automotive Actuators: Electromechanical actuators, Fluid-mechanical actuators, Electrical machines.

Text 2.	
Self-Study Component:	1. Illustrate and present the basic principles and applications of flex-fuel sensors in automotive. 2. Assess the performance, reliability, and durability of different actuators in various engine applications, considering factors like fuel type, engine load, and environmental conditions.

UNIT – IV	**8 Hours**

Digital Powertrain Control Systems: Introduction, Digital Engine control, Control modes for fuel Control, Discrete Time Idle Speed Control, EGR Control, Variable valve timing control, Direct Fuel Injection, Flex Fuel, Electronic Ignition Control, Integrated Engine Control System, Secondary Air Management, Evaporative Emissions Canister Purge, Automatic System Adjustment, System Diagnostics.
Text 1: Chapter 6.
Control Units: Operating conditions, Design, Data processing, Digital modules in the Control unit, Control unit software.
Text 2.

Self-Study Component:	1. Study and present Design procedures of Engine control system. 2. Explore the various Program control units available in automotive.

UNIT – V	**8 Hours**

Vehicle Communications: IVN, CAN, Local Interconnect Network, FlexRay IVN, MOST IVN, Vehicle to Infrastructure Communication, Vehicle-to-Cellular Infrastructure, Quadrature Phase Shifter and Phase Modulation (QPSR), Short-Range Wireless Communications, Satellite Vehicle Communication, GPS Navigation.
Electronic Safety-Related Systems: Airbag Safety Device, Blind Spot Detection, Automatic Collision Avoidance System.
Autonomous Vehicles: Automatic Parallel Parking System, Autonomous Vehicle Block Diagram.
Text 1: Chapter 9, Chapter 10 and Chapter 12.

Self-Study Component:	1. Study of Electronic Control System Diagnostics. 2. Explore Lane Departure Monitor and Tire Pressure Monitoring System. Present a brief report on the same.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Illustrate** an overview of electronic components, automotive components, subsystems, automotive networking and basics of Electronic Engine Control in today's automotive industry.	L2	PO1[L2]
CO2	Apply different automotive sensors and actuators in various electronic control systems in designing automotive system.	L5	PO4[L5]
CO3	Analyze the principles of networking in various modules of automotive systems and communication	L2, L4	PO1[L2] & PO5[L4]

	protocols for interfacing different electronics components, systems and mechanical parts.		
CO4	**Analyze** and **interpret** the different automotive control systems and Safety-Related Systems.	L4	PO4[L4] & PO5[L4]

Text Book(s):

1. William B. Ribbens, **"Understanding Automotive Electronics"**, 8th Edition, Elsevier Publishing. ISBN: 9780128104347.
2. Robert Bosch Gmbh (Ed.) **"Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive"**, 5th edition, John Wiley& Sons Inc., 2007. ISBN: 3658017848, 9783658017842.

Reference Book(s):

Nazamuz Zaman, **"Automotive Electronics Design Fundamentals"**, 2015, Springer Publications. ISBN: 978-3-319-17584-3.

Web and Video link(s):

1. https://youtu.be/BOP8qLQzhDc.
2. https://youtu.be/hs7bABMtOMI.
3. https://youtu.be/zzpOtJA-Rqw.

E-Books/Resources:

1. https://www.elsevier.com/books/understanding-automotive-electronics/ribbens/978-0-12-810434-7.
2. https://www.academia.edu/42742205/Bosch_Professional_Automotive_Information.

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5
#1	**3**				
#2				**2**	
#3	**3**				**1**
#4				**2**	**1**

FUTURE TECHNOLOGY

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – III

Course Code:	**P22MECEO334**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students:

- Understand the fundamental concepts and principles underlying emerging technologies such as artificial intelligence, biotechnology, nanotechnology, and quantum computing.
- Analyse the potential societal impacts of future technologies, including their effects on employment, ethics, privacy, and inequality.
- Explore the role of innovation and entrepreneurship in the development and adoption of future technologies.
- Evaluate the implications of future technologies on various industries, such as healthcare, transportation, communication, and energy.
- Develop critical thinking and problem-solving skills to anticipate and address challenges associated with the implementation of future technologies.

UNIT – I	**8 Hours**

Technology Road mapping Maturity Assessment: A Case Study in Energy Sector: Technology Planning, Technology Planning Maturity Assessment Model.

Technology Roadmap: Smart Apartments: Overview, Objective, ABC: Company Background, ABC Competitive Strategy, Market Analysis, Technology Road mapping Background, Methodology, Roadmap Elements, Political, Economic Drivers, Technology and Product Features, Technology and Product Features Gap Analysis, Quality Function Deployment (QFD), Technology Roadmap Timelines.

Text 1:1.1,1.2, 7.1-7.16.

Self-Study Component:	Flexible smart home design: Case study to design future smart home prototypes

UNIT – II	**8 Hours**

Technology Intelligence Map: Fast Charging for Electric Vehicles: Introduction, Literature Review, Methodology, XFC Forecast result, Technology Enablement Tipping Point.

Technology Intelligence Map: Lithium Metal Battery: Introduction, Literature Review, Methodology, Results and Discussion.

Text 1: 13.1-13.5,15.1-15.4.

Self-Study Component:	Discuss how many types of Electric Vehicles are there and name them?

UNIT – III	**8 Hours**

Technology Intelligence Map: Twitter and Currency: Introduction, Phase I: Finalizing Dataset, Phase II: Sentiment Analysis, Phase III: Regression.

Technology Intelligence Map: Space Tourism: Introduction, Literature Review, Methodology and Conclusion.

Text1: Chapter 16, Chapter 14.

Self-Study Component:	Analysis of Space Tourism's Place in the Space Economy, Patents, Key Players, Space Hotels, Main Source Markets, Challenges and Opportunities.

UNIT – IV	8 Hours
Technology Intelligence Map: Nanotubes: Introduction, Literature Review and Theoretical Background, Research Methodology and Data Analysis, Conclusions. **Technology Intelligence Map: Autonomous Car**: Introduction, Literature Review, Methodology, Factors That Impact Self-Driving Technology Based on SWOT, The Case Study of Google's Autonomous Vehicle Technology and Discussion. **Text 1.11.1-11.4,12.1-12.6.**	
Self-Study Component:	Case study of Polyvinylidene Fluoride Doping by Carbon Nanotubes.
UNIT – V	**8 Hours**
A Strategy Roadmap for Post-quantum Cryptography: Introduction, Methodology, Market and Business Drivers, Technology Features and Gap Analysis, Universities and the Affiliated Research Institutes, European Semiconductor Vendor, ESV's PQC Strategy **Text 1:4.1-4.7.**	
Self-Study Component:	Case study of IBM's quantum computer and envisioned applications.

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	***Analyze*** and understand the various fundamentals of fast charging technologies and battery technologies	L3	PO1[L3] & PO4[L3]
CO2	***Understand*** post-quantum cryptography standardization process, including criteria and stages of evaluation for PQC algorithms.	L2	PO2[L2]
CO3	***Infer*** the influence and consequence of different technological developments on battery, future space vehicles and autonomous vehicles.	L3	PO1[L3]
CO4	***Illustrate*** with case studies the best practices of successful technology road mapping initiatives across different industries	L3	PO3[L3] & PO5[L3]

Text Book(s):

3. **"Roadmapping Future Technologies, Products and Services"**, Tugrul U. Daim Editor, Springer,2021.ISBN-978-3-030-50501-1 ISBN-978-3-030-50502-8.

Reference Book(s):

5. **"Technology Road mapping and Development**", Olivier L. De Weck, Springer,2022.978- 3-030-88345-4 , ISBN: 978-3-030-88346-1

Web and Video link(s):

4. https://nptel.ac.in/courses/106106232
5. youtube.com/playlist?list=PLyqSpQzTE6M9spod-UH7Q69wQ3uRm5thr
6. digimat.in/nptel/courses/video/113105102/L58.html.

E-Books/Resources:

1. http://library.lol/main/0E74B109074DE5B82F5CA12EB4A8B666

Course Articulation Matrix (CAM)					
CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**
#1	**2**			**1**	
#2		**2**			
#3	**2**				
#4			**2**		**1**