SYLLABUS

(With effect from 2021-22)

Bachelor Degree
In

Electronics & Communication Engineering

V &VI Semester

Out Come Based Education
With
Choice Based Credit System

[National Education Policy Scheme]

P.E.S. College of Engineering, Mandya - 571 401, Karnataka
[An Autonomous Institution affiliated to VTU, Belagavi,
Grant – in – Aid Institution (Government of Karnataka),
Accredited by NBA (All UG Programs), NAAC and Approved by AICTE, New Delhi]

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VISION

"PESCE shall be a leading institution imparting quality Engineering and Management education developing creative and socially responsible professionals."

MISSION

- *Provide state of the art infrastructure, motivate the faculty to be proficient in their field of specialization and adopt best teaching-learning practices.*
- *Impart engineering and managerial skills through competent and committed faculty using outcome based educational curriculum.*
- *Inculcate professional ethics, leadership qualities and entrepreneurial skills to meet the societal needs.*
- *Promote research, product development and industry-institution interaction.*

QUALITY POLICY

Highly committed in providing quality, concurrent technical education and continuously striving to meet expectations of stake holders.

CORE VALUES

***P**rofessionalism*
***E**mpathy*
***S**ynergy*
***C**ommitment*
***E**thics*

Department of Electronics and Communication Engineering

The department of Electronics and Communication Engineering was incepted in 1967 with an undergraduate program in Electronics and Communication Engineering. Initially, the program had an intake of 60 students, which increased to 120 in 2012, and further increased to 180 in 2019. Almost 200 students graduate every year, and the long journey of 50 years has seen satisfactory contributions to society, the nation, and the world. The alumni of this department have a strong global presence, making their alma mater proud in every sector they represent.

The department started its PG program in 2012 in the specializations of VLSI design and embedded systems. Equipped with well qualified and dedicated faculty, the department has a focus on VLSI design, embedded systems, and image processing. The quality of teaching and training has yielded a high growth rate of placement at various organizations. The large number of candidates pursuing research programs (M.Sc. and Ph.D.) is a true testimonial to the research potential of the department. The department is recognized as a research centre by VTU, and Mysore University offers a part-time and full-time Ph.D. Program.

Vision

The department of E & C would end eavour to create a pool of Engineers who would be extremely competent technically, ethically strong also fulfil their obligation in terms of social responsibility.

Mission

- M1: Adopt the best pedagogical methods and provide the best facility, infrastructure and an ambience Conducive to imbibe technical knowledge and practicing ethics.
- M2: Group and individual exercises to inculcate habit of analytical and strategic thinking to help the Students to develop creative thinking and instill team skills
- M3: MoUs and Sponsored projects with industry and R & D organizations for collaborative learning
- M4: Enabling and encouraging students for continuing education and moulding them for life-long Learning process

Program Educational Objectives (PEOs)

- **PEO1:** Graduates to exhibit knowledge in mathematics, engineering fundamentals applied to Electronics and Communication Engineering for professional achievement in industry, research and academia
- **PEO2:** Graduates to identify, analyse and apply engineering concepts for design of Electronics and Communication Engineering systems and demonstrate multidisciplinary expertise to handle societal needs and meet contemporary requirements
- **PEO3:** Graduates to perform with leadership qualities, team spirit, management skills, attitude and ethics need for successful career, sustained learning and entrepreneurship.

Program Outcomes (POs)

- **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
- **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
- **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

Electronics and Communication Engineering Graduates will be able to

- **PSO1:** An ability to understand the basic concepts in Electronics and Communication Engineering and to apply them in the design and implementation of Electronics and Communication Systems.
- **PSO2:** An ability to solve complex problems in Electronics and Communication Engineering, using latest hardware and software tools, along with analytical skills to arrive at appropriate solutions.

Bachelor of Engineering (V –Semester)											
Sl. No.	Course Code	Course Title	Teaching Department	Hrs / Week				Credits	Examination Marks		
				L	T*	P	PJ		CIE	SEE	Total
1	P21 EC 501	Innovation Entrepreneurship and Management	EC	3	-	-	-	3	50	50	100
2	P21 EC 502	Digital CMOS VLSI Design	EC	3	-	-	-	3	50	50	100
3	P21 EC 503X	Professional Elective Course - I	EC	3	-	-	-	3	50	50	100
4	P21 EC 504	Digital Signal Processing	EC	3	-	2	-	4	50	50	100
5	P21 ECO505X	Open Elective – I	EC	3	-	-	-	3	50	50	100
6	P21 EC L506	Circuit Simulation Laboratory	EC	-	-	2	-	1	50	50	100
7	P21INT507	Internship - II	EC	-	-	-	-	2	-	100	100
8	P21HSMC508	Employability Enhancement Skills – V	HSMC	1	-	-	-	1	50	50	100
9	P21UHV509	Social Connect and Responsibility	EC	1	-	-	-	1	50	50	100
Total								**21**			

Professional Elective Course – I (P21EC503X)	
Course Code	**Course Title**
P21EC5031	Fundamentals of object oriented Language and Database Concepts
P21EC5032	System Verilog
P21EC5033	Control System
P21EC5034	ARM Processors

Open Elective – I(P21ECO505X)	
Course Code	**Course Title**
P21EC O5051	E-Waste Management
P21EC O5052	Principles of Communication Systems
P21EC O5053	Biometrics
P21EC O5054	Sensors and IOT

Bachelor of Engineering (VI –Semester)											
Sl. No.	Course Code	Course Title	Teaching Department	Hrs / Week				Credits	Examination Marks		
				L	T*	P	PJ		CIE	SEE	Total
1	P21EC601	Analog CMOS VLSI Design	EC	3	-	-	-	3	50	50	100
2	P21EC602X	Professional Elective Course – II	EC	3	-	-	-	3	50	50	100
3	P21EC603X	Professional Elective Course - III	EC	3	-	-	-	3	50	50	100
4	P21EC604	Microwave and Antenna	EC	3	-	2	-	4	50	50	100
5	P21ECO605X	Open Elective – II	EC	3	-	-	-	3	50	50	100
6	P21ECL606	Analog and Digital VLSI Design Laboratory	EC	-	-	2	-	1	50	50	100
7	P21ECMP607	Mini – Project	EC	-	-	2	2	2	50	50	100
8	P21HSMC608	Employability Enhancement Skills - VI	HSMC	1	-	-	-	1	50	50	100
9	P21UHV609	Universal Human Values and Professional Ethics	XX	1	-	-	-	1	50	50	100
Total								**21**			

Professional Elective Course – II (P21EC602X)	
Course Code	**Course Title**
P21EC6021	ITC and Multimedia Communications
P21EC6022	Real Time Signal Processing using Simulink
P21EC6023	Embedded Systems
P21EC6024	Operating System
P21EC6025	Fundamentals of Network Communication

Professional Elective Course – III (P21EC603X)	
Course Code	**Course Title**
P21EC6031	Computer Organization
P21EC6032	Digital Image Processing
P21EC6033	Design for Testability
P21EC6034	Artificial Intelligence and Machine Learning using VLSI

Open Elective – II (P21ECO605X)	
Course Code	**Course Title**
P21ECO6051	Electronic Instrumentation
P21ECO6052	Introduction to Embedded Systems
P21ECO6053	Introduction to Image Processing
P21ECO6054	Automotive Electronics

***Allot Tutorial as per the course requirement subjected to the credits allotted.**

L –Lecture, T – Tutorial, P- Practical/ Drawing, CIE: Continuous Internal Evaluation, SEE: Semester End Examination

Innovation, Entrepreneurship and Management [As per Choice Based Credit System (CBCS) & OBE Scheme] **SEMESTER – V**			
Course Code:	**P21EC501**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives:.

1. Relate the role and importance of innovation in economic growth, skills of innovator, types of innovation and output forms of innovation.
2. Understand various ways to create and manage intellectual property and prepare innovation proposal.
3. Understand the entrepreneurial development process and recognize the core role of creativity and innovation in managing the entrepreneurial process effectively.
4. Understand the fundamental concepts and principles of management, including the basic roles, skill,and functions of management.
5. Understand the procedure of creating an ownership and its types.
6. Express the meaning of Professional Ethics, its importance and needs.

UNIT – I	**8 Hours**

Introduction to Innovation and Innovator: Introduction, understanding Innovation, Creativity and Research, Role of Innovation in economic growth of country, companies and community, phases of innovation journey, Roles of Innovator.

Text 1: Chapter 1 to 5

Self-study component:	Prepare a Case study of An Innovator: How did he/she find the problem, thought about a solution and steps/situations came across during implementation.

UNIT – II	**8 Hours**

Innovator Skills and Innovation: Introduction to Innovative Skills, Types of Innovation, Introduction to patents and IP, preparing an innovation proposal Pitching an innovation proposal, Sustaining innovation.

Text 1: Chapter 6 to 13

Self-study component:	Prepare a case study of an entrepreneur around you.

UNIT – III	**8 Hours**

Entrepreneurship and Entrepreneurs: Evolution of the concept of Entrepreneur, Characteristics of an Entrepreneur, Distinction between an Entrepreneur & a Manager, Functions of an Entrepreneur, Types of Entrepreneur. Concept of Entrepreneurship, Growth of Entrepreneurship in India, Role of Entrepreneurship in Economic Development.

Text 2: 1.1 to 1.10, 2.1 to 2.3

Self-study component:	Prepare a Case Study of an Entrepreneur / an Enterpriser or an Enterprise.

UNIT – IV	**8 Hours**

Management and Business Ownership: Fundamentals of Management: Meaning of Management, Management as Science, Art & Profession, Importance of Management, Scope of Management, Functions of Management, Management Process, Principles of Management. Forms of Business Ownership: Sole Proprietorship, Partnership, Company, Cooperative, Selection of Appropriate Form of Ownership Structure.

Text 2: 24.1 to 24.9 & 18.1 to 18.5

Self-study component:	Being in different positions as an employee: Understanding Self, Self-Management& Understanding others for Effective Relationships and Communication.

UNIT – V	**8 Hours**

Engineering and Professional Ethics: Making a Case: Introduction, Role Morality, What is a Profession?, Professional Ethics, The NSPE Board of Ethical Review, Engineering Ethics as Preventive Ethics

Honesty: Introduction, Ways of Misusing Truth, Why is Dishonesty Wrong?

International Engineering Professionalism: Introduction, Problems in International Professionalism, Problems in Interpreting and Applying the Codes, Striking a Balance, Guidelines for Interpreting the Codes: Human Rights, Avoiding Paternalism and Exploitation and Applying the Golden Rule, Bribery-Extortion-Grease Payments and Gifts.

Text 3: 1.1 to 1.6, 6.1 to 6.3 & 10.1 to 10.8

Self-study component:	Survey and Study the importance of Professional Ethics

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) withBTL**
CO1	Identify the innovation phases and skills required for innovation	Understand and Apply	PO1(L2)
CO2	Examine the role of management in an organization	Apply	PO1(L3)
CO3	Analyze entrepreneurship with necessary theories	Analyze	PO1(L2), PO2(L3)
CO4	Distinguish among various types of business ownership and selecting appropriate form of ownership structure.	Analyze	PO1(L2), PO2(L3)
CO5	Interpret the role of professional ethics including international engineering professionalism	Understand and apply	PO1(L2), PO6(L2), PO8(L3)

Text Book(s):

1. "A Conversation with the Innovator in You", SudeendraKoushik and Pragya Dixit, Kindle Direct Publishing, Amazon, 2017. ISBN-10: 1520512716, ISBN-13: 978-152051271.
2. "Entrepreneurial Development", by Dr S S Khanka, S Chand & Company Ltd. ISBN- 10: 8121918014; ISBN-13: 978-8121918015.
3. "Engineering Ethics" (2nd edition), Charles E. Harris, Michel S. Pritchard and Michel J. Rabins, Thomson Wadsworth Asia Pte Ltd, 2003. ISBN: 981-243-676-6.

Reference Book(s):

1. "Debono, Edward: Six thinking hats", Penguin Books (2000).ISBN 10: 0140296662 / ISBN 13: 9780140296662.
2. "Entrepreneurship" by Robert D Hisrich, Micheal P Peters, Dean A Shepherd- 6/e, TataMcGraw – Hill Companies.ISBN-10: 0078029198.
3. "Principles and practice of management" – L. M. Prasad.ISBN-13: 9789351610502.

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	2												2	
#2	3												3	
#3	2	3											2	3
#4	2	3											2	3
#5	2					2		3					2	

Digital CMOS VLSI Design

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – V

Course Code:	**P21EC502**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. Discuss the VLSI Design Flow, MOS Structure, and the MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current –Voltage Characteristics.
2. Analyze the MOS Inverters, Static Characteristics, Switching Characteristics and Interconnect Effects.
3. Examine the static and dynamic characteristics of Combinational MOS logic circuits and Pass Transistor Circuits.
4. Explain the SR Latch Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High–Performance Dynamic CMOS Circuits.
5. Examine the MOS Technology and MOS circuit design processes.

UNIT – I — **8 Hours**

Introduction: Historical Perspective, VLSI Design Flow,
MOS Transistor: The Metal Oxide Semiconductor(MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor (MOSFET), MOSFET Current –Voltage Characteristics.
Text 1:– 1.1, 1.5, 3.1 to 3.4.

Self-study component:	1. Design hierarchy 2. VLSI Design Styles

UNIT – II — **8 Hours**

MOS Transistor: MOSFET Scaling and Small geometry effects, MOSFET Capacitance
MOS Inverters, Static Characteristics: Introduction, CMOS Inverter: Calculation of V_{IL}, V_{IH}, andV_{th}, Design of CMOS Inverter, Supply Voltage Scaling in CMOS Inverter.
Text 1:–3.5, 3.6, 5.1, 5.4,

Self-study component:	1. Super buffer Design. 2. Switching Power Dissipation of CMOS Inverter

UNIT – III — **8 Hours**

Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definitions, Calculation of Interconnect Delay.
Combinational MOS Logic Circuits: Introduction, CMOS Logic Circuits, Complex Logic Circuits, Basic Principles of Pass Transistor Circuits, CMOS Transmission Gates(Pass Gates).
Text 1:– 6.1, 6.2, 6.6, 7.1, 7.3, 7.4, 7.5, 9.2

Self-study component:	Modeling of MOS Transistor using SPICE**:** Know about MODEL statement in SPICE. Plot O/P characteristics of N-MOS and P-MOS transistors and C-MOS inverter using, LEVEL-1 and LEVEL-2 model in SPICE and Scilab/Math lab.

UNIT – IV	8 Hours

Sequential MOS Logic Circuits: Introduction, SR Latch Circuit
Dynamic Logic Circuits: Introduction, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High–Performance Dynamic CMOS Circuits (Including only Domino CMOS logic).
Text 1:– 8.1, 8.3, 9.1, 9.3 to 9.6

Self-study component:	1. Clocked Latch and Flip-Flop Circuits 2. CMOS D-Latch and Edge Triggered Flip-Flop

UNIT – V	8 Hours

Introduction to MOS Technology:nMOS Fabrication, CMOS Fabrication, Thermal Aspects of Processing, Latch-up in CMOS Circuits,.
MOS Circuits Design Processes:MOS Layers, Design rules and Layout, General Observations on the Design rules.
Text 2:–1.7,1.8,1.9, 2.13, 3.1, 3.3,3.4.

Self-study component:	1. BiCMOS Technology 2. BiMOS Circuits Design Processes

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Discuss and Demonstrate** the VLSI Design Flow, working of MOS Circuits, CMOS Circuits, MOS Technology and MOS circuit design processes.	Understand Apply	PO1(L3)
CO2	**Interpret** the working of MOSFET, MOS Technology and MOS circuit design processes.	Apply	PO1 (L3)
CO3	**Examine** the MOSFET, MOS circuits and CMOS circuits.	Analyze	PO2 (L4)
CO4	**Design** the Combinational, Sequential and Dynamic circuits based on MOSFET for the given specifications.	Create	PO2(L2), PO3 (L6)
CO5	**Investigate** the Modeling of a MOS transistors and its circuits using modern simulation tools.	Create	PO5, PO9,PO12 (L6)

Text Book(s):

1. **"CMOS Digital Integrated Circuits Analysis and Design",** Sung Mo Kang, Yusuf Leblebici, 3rd edition, McGraw Hill Education 2003, ISBN-13:978-0-07-053077-5, ISBN-10:0-07-053077-7.
2. **"Basic VLSI Design"**, Douglas A. Pucknell, Kamran Eshraghian, 3rd edition 2006, PHI, ISBN: 978-81-203-0986-9.

Reference Book(s):

1. **"Introduction to VLSI Circuits and Systems"**, John .P. Uyemura, John Wiley, 3rd edition 2002. ISBN: 978-81-265-0915-7
2. **"Principles of CMOS VLSI Design",** Neil. H. E. Weste, Kamran Eshraghian, 3rd edition, Pearson Education 2005, ISBN:978-81-317-6467-1.

Web and Video link(s):

1. https://archive.nptel.ac.in/courses/108/107/108107129/
2. https://www.youtube.com/watch?v=Iv4Cj2A3ldw&list=PLuv3GM6-gsE3npYPJJDnEF3pdiHZT6Kj3&index=3

E-Books/Resources:
http://brharnetc.edu.in/br/wp-content/uploads/2018/11/31.pdf

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2	3												3	
#3		3												3
#4		2	3											2
#5					2				2			2		

Professional Elective Course – I

Fundamentals of Object Oriented Language and Database Concepts

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – V

Course Code:	**P21EC5031**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. Explain the significance of object oriented concepts
2. Describe the concept of class, objects and methods in Java
3. Apply the concepts of inheritance and interfaces in Java
4. Illustrate usage of packages, string handling and exception handling in Java
5. State the importance of DBMS and explain how DBMS is better than traditional File Processing Systems.
6. Analyze the basic structure of Database and recognize the different views of the database.
7. Draw and Investigate Data Flow and Entity Relationship Diagrams.
8. Analyze and use Relational Data Model, while comparing with other data models.
9. Formulate data retrieval queries in SQL and the Relational Algebra and Calculus.

UNIT – I	**8 Hours**

Fundamentals of Object Oriented Programming: Introduction, Object oriented paradigm, Basics concepts of object oriented programming, Benefits of object oriented programming, Applications of object oriented programming.
Java: Features, Simple Java Program, Java Program Structure, Data types, Operators overview
Decision Making and Branching: if, if else, else if ladder, nesting of if else statements, switch
Decision Making and Looping: do, while, for, Jumps in loops.
Text 1:1.1-1.5, 2.2, 3.2, 3.5, 4.4, 4.5, 5.1-5.9, 6.2-6.7, 7.2-7.5.

Self-study component:	How Java is different from C and C++, Java environment.

UNIT – II	**8 Hours**

Classes, Objects and Methods: Introduction, Defining a class, Fields declaration, Methods declaration, Creating objects, Accessing class members, Constructors, Method Overloading, Static members, Nesting ofMethods, Inheritance, Overriding methods.
Arrays: Creating array, 1D array and 2D array.
Text 1:8.1-8.12, 9.2-9.3.

Self-study component:	Understand the concept of Inheritance: Defining subclass, Subclass Constructor.

UNIT – III	**8 Hours**

Strings: String Arrays, String Methods
Interfaces: Introduction, Defining interfaces, Extending interfaces, implementing interfaces
Packages: Introduction, Java API packages, Using System packages, Naming conventions, creating packages, accessing a package, using a package, adding a class to a package.
Text 1: 9.5, 10.1-10.4, 11.1-11.8.

Self-study component:	Discuss the Accessing interface variables, String buffer class.

UNIT – IV	8 Hours

Database and Database users: Introduction, An example, Characteristics of the database approach, Actors on the scene, Workers behind the scene.
Database system concepts and architecture: Database models, Schema and Instances, Three schema architecture and data independence, Database languages and interfaces.
Data Modeling using ER Model: Using High level conceptual data models for database design, Entity types, Entity sets, Attributes and keys, Relationship types, Relationship sets, Roles and structural constraints.
Text 2:1.1-1.5, 2.1-2.3, 7.1, 7.3, 7.4

Self-study component:	Identify the Advantages of using DBMS approach.

UNIT – V	8 Hours

Basics SQL: SQL Data Definition and Data types, Specifying constraints in SQL, Basic Retrieval Queries in SQL, Insert, Delete and Update statements in SQL.
Relational Model and Relational Database Constraints: Relational Model concepts, Relational data model constraints and relational database schemas, Update operations, Transactions and dealing with constraint violations.
Text 2: 3.1-3.3, 4.1-4.4

Self-study component:	Discuss the Additional features of SQL, Views in SQL.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Apply** basic knowledge of programming in understanding concepts and syntax of Java.	**L4, L2**	**PO1 , PO5**
CO2	**Analyze** Java programs, debug Java programs.	**L3, L2**	**PO2 ,PO5**
CO3	**Implement** the various concepts of Java features in the development of Java Program.	**L3, L4**	**PO3 , PO5**
CO4	**Identify** the basic concepts and various data model used in database design ER modeling concepts and architecture use.	**L1, L1**	**PO1, PO5**
CO5	Apply relational database theory to **Design** queries using SQL.	**L3, L3**	**PO3, PO5**

Text Book(s):

1. **"Programming With JAVA":** A Primer, E Balagurusamy, 6th edition Tata McGraw Hill. ISBN 13: 978-93-5316-233-7, ISBN 10:-93-5316-233-5
2. **"Fundamentals of Database Systems"** – Elmasri and Navathe, 6th edition, Addison-Wesley, 2011. ISBN 10: 0-136-08620-9 ISBN 13: 978-0-136-08620-8

Reference Book(s):

1. **"The Complete Reference JAVA, J2SE",** Herbert Schildt, 6th edition, TMH, 2010.*ISBN*: 0070598789.
2. **"C++ Primer",** Stanley B. Lippman, JoseeLajoie, Barbara E. Moo, 5th edition, Addison Wesley, 2012. ISBN-13: 978-0-321-71411-4, ISBN-10: 0-321-71411-3.
3. **"Database Management Systems"** Raghu Ramakrishnan and Johannes Gehrke – 3rd edition, McGraw-Hill Education(India) Edition 2014. ISBN 0-07-246563-8, ISBN -0-07-115110-9.
4. **"Data Base System Concepts"** – Silberschatz, Korth and Sudharshan, 5th edition, Mc-GrawHill, 2006 *ISBN* 0072958863, 9780072958867

WebandVideolink(s):

1. DBMS – SWAYAM - https://nptel.ac.in/courses/106/105/106105175/
2. Java Programming - https://nptel.ac.in/courses/106/105/106105191/

E-Books/Resources:

1. **https://books.google.co.in/books?id=a9q5AwAAQBAJ**
2. **https://docs.ccsu.edu/curriculumsheets/ChadTest.pdf**

https://gfgc.kar.nic.in/sirmv-science/GenericDocHandler/138-a2973dc6-c024-4d81-be6d-5c3344f232ce.pdf

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3				1								3	
#2		3			2									3
#3			3		3									
#4	3				1								3	
#5			3		2									

System Verilog

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – V

Course Code:	**P21EC5032**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. Develop an understanding of the System Verilog language constructs.
2. Introduce the facilities and features of System Verilog for unified Design, testing and verification.
3. Introduce the programming approach for testing and verification.
4. Provide framework of System Verilog for functional coverage.

UNIT – I **8 Hours**

Verification Guidelines: The Verification Process, Basic Test Bench Functionality, Directed testing, Methodology Basics, Constrained Random Stimulus, Functional Coverage, Test bench Components, Layered Test bench.

Data Types: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing a Storage Type, Creating New Types with typed of, Creating User-Defined Structures, Enumerated Types, Constants, Strings, Expression Width.

Procedural Statements and Routines: Procedural Statements, Tasks, Functions, and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values.

Text 1: 1.1,1.3-1.10,2.1-2.16, 3.1-3.7.

Self-study component:	Synthesizable constructs in system Verilog (Refer: Synthesizing SystemVerilog Busting the Myth that SystemVerilog is only for Verification by Stuart Sutherland and Don Mills)

UNIT – II **8 Hours**

Basic OOPs: Your First Class, Where to Define a Class, Creating New Objects, Object De allocation, Using Objects, Class methods, Defining methods outside of the class.Static Variables vs. Global Variables, Scoping Rules, Using One Class inside Another, Understanding Dynamic Objects, Copying Objects, Public vs. Private Straying off Course, Building a Test bench.

Text 1: 5.3-5.18.

Self-study component:	System Verilog Macro's and their usage

UNIT – III **8 Hours**

Randomization and Constraints: Introduction, What to Randomize, Randomization in System Verilog, Constraint Details, Solution Probabilities, Controlling Multiple Constraint Blocks, Valid Constraints, In-line Constraints. The pre_randomize and post_randomize Functions, Random Number Functions, Constraints Tips and Techniques, Common Randomization Problems. Iterative and Array Constraints, Atomic Stimulus Generation vs. Scenario Generation, Random Control, Random Number Generators, Random Device Configuration.

Text 1: 6.1-6.17.

Self-study component:	Methods: get_randstate and set_randstate

UNIT – IV **8 Hours**

Threads and Inter Process Communication: Working with Threads, Disabling Threads, Interprocess Communication, Events, Semaphores, Mailboxes, Building a Testbench with Threads and IPC.

Text 1: 7.1-7.7.

Self-study component:	Built in class process and related methods to control the process	
UNIT – V		**8 Hours**

Functional Coverage: Gathering Coverage Data, Coverage Types, Functional Coverage Strategies, Simple functional Coverage examples, Anatomy of a cover group, triggering a cover group.Data Sampling, Cross coverage, Generic cover groups, Coverage Options, Analyzing Coverage Data, and Measuring Coverage Statistics during simulation, System Verilog Assertions.
Text 1: 9.1-9.12, 4.8.

Self-study component:	Functional coverage constructs and functional coverage flow

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with **Action verbs** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO#) with BTL**
CO1	**Understand** the System Verilog language constructs.	Understand, Apply	**PO1, PO2, PO3 (L1)**
CO2	**Understand** the System Verilog OOPs facilities and framework for the verification.	Apply , Analyze	**PO2, PO3 (L1)**
CO3	**Develop** programs by applying the System Verilog facilities and framework.	Understand , Apply	**PO1, PO3, PO4 (L4)**
CO4	Explore and **understandmodern software tools** to perform different operations in System Verilog.	Apply, Analyze	**PO1, PO2, PO5 (L3)**
CO5	**Develop** the capability to learn on your own individually and in group to explore advanced technologies in system Verilog.	Understand , Apply	**PO9, PO12 (L4)**

Text Book(s):

1. **"System Verilog for Verification: A Guide to Learning the Testbench Language Features",** Chris Spear, Springer-Verlag New York, Inc, 3rd edition, ISBN 978-1-4614-0714-0, 2012.

Reference Book(s):

1. **"Hardware Verification with System Verilog (An Object Oriented Framework)",** Mike Mintz and Robert Ekehndal, Springer, USA, ISBN 0-387-71738-2, 2007.
2. **"SystemVerilog For Design A Guide to Using SystemVerilog for Hardware Design and Modeling",** Stuart Sutherland, Simon Davidmann and Peter Falke, Springer, USA, ISBN 9781475766820, 1475766823, 2013.

Web and Video link(s):

E-Books/Resources:

1. https://www.kobo.com/in/en/ebook/systemverilog-for-verification
2. https://www.chipverify.com/systemverilog/systemverilog-tutorial

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	1	2	1										1	2
#2		3	1											3
#3	1		2	1									1	
#4	2	2			2								2	2
#5									2			2		

Control Systems
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – V

Course Code:	**P21EC5033**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. Determine the mathematical transfer function models of electrical system, mechanical system and analogous system.
2. Determine the transfer function from the block diagrams and signal flow graph techniques of different system.
3. Analyze the performance of different systems by determining the time Response specifications.
4. Analyze the stability of different systems by analytical and graphical means.(By sketching plots)
5. Discuss the concepts of state models for different electrical systems.

UNIT – I	**8 Hours**

Fundamental Concepts of Control Systems: Basic definitions of control systems, Classification, Open loop and closed loop systems,
Modeling of Systems: Differential equations of physical systems,Determinations of transfer function models for Electrical, Mechanical and Analogous systems.
Block Diagrams and Signal Flow Graphs: Transfer functions, Block diagram algebra, Signal Flow graphs (State variable formulation excluded).
Text 1: 1.1, 2.1, 2.2, 2.4, 2.5, 2.6, 2.7.

Self-study component:	1. Develop the Block diagram for field and armature controlled D.C. Servomotors. 2. Develop the system equations and TF model for a seated human body with applied force.

UNIT – II	**8 Hours**

Time Domain (Transient and Steady State Response) Analysis of Feedback Control Systems: Standard test signals, Unit step response of First and second order systems.
Time Response Specifications: Transient response specifications of second order systems, steady state errors and static error constants.
Text 1: 2.4, 2.5, 2.6, 2.7, 5.1, 5.2, 5.3, 5.4, 5.5

Self-study component:	1. Determine the transient response specifications of second order RLC systems for R=1000 ohms, L=1 Henry and C=2μF.

UNIT – III	**8 Hours**

Stability Analysis: Concepts of stability, asymptotic stability, necessary conditions for stability, Routh-Hurwitz stability criterion, Routh's tabulation, special cases when Routh's tabulation terminates prematurely.
Root Locus Techniques: The root locus concepts, summary of general rules for constructing Root Loci, Stability analysis.
Text 1: 6.1, 6.2, 6.4, 6.5, 6.6, 7.1, 7.2, 7.3

Self-study component:	1. Write the MATLAB program to draw the Root Locus diagrams of open loop transfer function of different systems. **(Refer Text 2)**

UNIT – IV	8 Hours

Frequency-Response Analysis:Stability in the frequency domain: Introduction to frequency domain analysis, Experimental determination of transfer functions in bode plots. Assessment of relative stability using bode Plots.

Polar Plot: Introduction to Polar plot and Nyquist plots, Nyquist stability criterion, Stability analysis using polar plot, Numerical problems.

Text 1: 8.1, 8.4, 8.5, 8.6, 9.1, 9.2, 9.3, 9.4.

Self-study component:	1. Write the MATLAB program to draw the Bode diagrams of open loop transfer function of different systems. **(Refer Text 2)** 2. Frequency response specifications- resonant peak, resonant frequency and bandwidth.

UNIT – V	8 Hours

Introduction to State variable analysis: Concepts of state, state variable and state models for electrical systems, Controllability and observability, Derivation of transfer functions from the state model, Solution of state equations.

Text 1: 12.1, 12.2, 12.3, 12.6, 12.7

Self-study component:	1. Obtain the time response for different state models

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with Action verbs for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO#) with BTL
CO1	**Use the** knowledge of mathematics to determine the Transfer function of systems.	Apply	PO1(L3)
CO2	**Analyze** the stability of a system using different techniques	Analyze	PO1(L2),PO2(L3)
CO3	**Analyze** the response of the system in time and frequency domain and state variable techniques	Analyze	PO1(L2),PO2(L3)
CO4	**Develop** the mathematical models using different techniques of state variables.	Create	PO2(L2),PO3(L3)
CO5	**Design** using the linear control system using MATLAB software.	Create	PO3(L3), PO5(L3), PO9(L3)

Text Book(s):

1. **"Control Systems Engineering",** I. J. Nagarath and M. Gopal, New Age International (P) Limited, Publishers, 4th edition – 2005, ISBN 10:8122420087; ISBN 13: 9788122420081.
2. **"Modern Control Engineering",** K. Ogata, Pearson Education Asia/ PHI, 4th edition, 2002. ISBN 0-13-043245-8.

Reference Book(s):

1. **"Automatic Control Systems",** Benjamin C. Kuo, John Wiley India Pvt. Ltd., 8th edition, 2008, ISBN 978-81-203-4010-7
2. **"Feedback Control System Analysis and Synthesis",** J. J. D'Azzo and C. H. Houpis McGraw Hill, International student Edition, ISBN 10: 0070161755 / ISBN 13: 9780070161757.

Web and Video link(s):

1. NPTEL course on "Introduction to System and Control" by Prof Ramakrishna Pasumarthy, IIT Madras https://nptel.ac.in/courses/108/106/108106098/

E-Books/Resources:

1. https://www.google.co.in/books/edition/Control_Systems_As_Per_Latest_Jntu_Sylla/VMBWs_8hyBgC?hl=en&gbpv=1&dq=control+systems+by+ij+nagrath&printsec=frontcover
2. http://libgen.rs/book/index.php?md5=A9371B939B494BC8D81F845420939513

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2	2	3											2	3
#3	2	3											2	3
#4		2	3											2
#5			3		3				3					

ARM Processor [As per Choice Based Credit System (CBCS) & OBE Scheme] **SEMESTER – V**			
Course Code:	**P21EC5034**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. Provide the knowledge of general architecture of ARM Cortex-M3 processor.
2. Understand the Instruction set of Cortex-M3 processor.
3. Understand Memory system, exceptions and interrupt control.
4. Provide the knowledge of fault interrupt behavior, Cortex-M3 and Exceptions Programming.
5. Provide the knowledge of Advanced Programming Features and System Behavior.

UNIT – I	**8 Hours**

Introduction: What Is the ARM Cortex-M3 Processor?, Background of ARM and ARM Architecture, Instruction Set Development, The Thumb-2 Technology and Instruction Set Architecture(ISA),Cortex-M3 Processor Applications.

Overview of the Cortex-M3: Fundamentals, Registers, Operation Modes, The Built-In Nested Vectored Interrupt Controller, The Memory Map, The Bus Interface, The Memory Protection Unit, The Instruction Set, Interrupts and Exceptions, Debugging Support.

Text1:1.1 - 1.5, 2.1 - 2.10.

Self-study component:	1. Study the C programming for advanced Cortex processors. 2. Discuss the various advantages of using Cortex-M3.

UNIT – II	**8 Hours**

Cortex-M3 Basics: Registers, Special Registers, Operation Mode, Exceptions and Interrupts, Vector Tables, Stack Memory Operations, Reset Sequence.

Instruction Sets: Assembly Basics, Instruction List, Instruction Descriptions.

Text1:3.1 - 3.7, 4.1 - 4.3

Self-study component:	1. Identify the applications of stack operation. 2. Understand several useful instructions in Cortex-M3..

UNIT – III	**8 Hours**

Memory Systems: Memory System Features Overview, Memory Maps, Memory Access Attributes, Default Memory Access Permissions, Bit-Band Operations, Unaligned Transfers, Exclusive Accesses, Endian Mode.

Cortex-M3 Implementation Overview: The Pipeline, A Detailed Block Diagram, Bus Interfaces on the Cortex-M3, Other Interfaces on the Cortex-M3, The External Private Peripheral Bus, Typical Connections, Reset types and Reset Signals.

Text1:5.1 - 5.8, 6.1 - 6.7

Self-study component:	1. Identify the advantages and disadvantages of big Edian and little Endian processor. 2. Identify the different reset signals in Cortex-M3.

UNIT – IV	**8 Hours**

Exceptions: Exception Types, Definitions of Priority, Vector Tables, Interrupt Inputs and Pending Behavior, Fault Exceptions.

The NVIC and Interrupt Control: NVIC Overview, the Basic Interrupt Configuration, Example Procedures in Setting up an Interrupt, Software Interrupts.

Interrupt Behavior: Interrupt/Exception Sequences, Exception Exits, Nested Interrupts, Tail-Chaining Interrupts, Late Arrivals, More on the Exception Return Value, Interrupt Latency, Faults Related to Interrupts.
Text1:7.1 - 7.5, 8.1 - 8.4, 9.1 - 9.8

Self-study component:	1. Discuss the applications of Systick timer. 2. Understand the concept of supervisor calls and pendable service call

UNIT – V	**8 Hours**

Cortex-M3 Programming: Overview, A Typical Development Flow, CMSIS, using Assembly, Using Exclusive Access for Semaphores, Using Bit Band for Semaphores, Working with Bit Field Extract and Table Branch.
Exceptions Programming: Using Interrupts, Exception/Interrupt Handlers, Software Interrupts, Example of Vector Table Relocation, Using SVC, SVC Example: Use for text message output Functions, Using SVC with C.
Advanced Programming Features and System Behavior: Running a System with Two Separate Stacks, Double-Word Stack Alignment, Nonbase Thread Enable.
Text1:10.1 - 10.2, 10.4 - 10.8, 11.1 - 11.7, 12.1 - 12.3

Self-study component:	1. Give an example of a simple C program using Real view development site. 2. Discuss what happens during lockup.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Apply** the knowledge of basic Controller to understand the architecture, instruction set, addressing modes and other features of ARM cortex-M3 processor.	**Understand and Apply**	**PO1(L1)**
CO2	**Classify** the different peripheral components associated with ARM cortex-M3 processor.	**Analyze**	**PO2(L2)**
CO3	**Interpret** theARMprocessorbased applications, interruptsandexceptions.	**Evaluate**	**PO2(L2)**
CO4	**Develop** the embedded system applications for the given specification using theBasic knowledge of cortex M-3 and using 'C' Programming.	**Create**	**PO3(L2)**
CO5	ARM applications using Modern tools.	**Create**	**PO5(L2)**

Text Book(s):

1. **"The Definitive Guide to the ARM Cortex-M3" by JosephYiu, 2ndedition, Newnes, (Elsevier), ISBN:978-0-7506-8534-4,2007.**

Reference Book(s):

1. **"**ARM Assembly Language Fundamentals and Techniques", William HohlandChristopherHinds, 2ndedition, ISBN 9781482229851, 2014, CRC (TaylorandFrancis)
2. "ARMSystem-On-Chip Architecture" SteveFurber, 2ndedition, Pearson, ISBN: 9788131708408, 8131708403, 2015.

Web and Video link(s):

1. NPTELCourse by Prof.IndranilSenguptaDept.of Computer Science and Engineering IIT Kharagpur, https://nptel.ac.in/courses/106/105/106105193/

E-Books/Resources:

1. http://centaur.sch.bme.hu/~holcsik_t/sem/The%20Definitive%20Guide%20to%20the%20ARM%20Cortex-M3.pdf

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2		3												3
#3		2												2
#4			2											
#5					2									

Digital Signal Processing [As per Choice Based Credit System (CBCS) & OBE Scheme] **SEMESTER – V**			
Course Code:	**P21EC504**	**Credits:**	**04**
Teaching Hours/Week (L:T:P):	**3:0:2**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. Provide the knowledge of DFT/ IDFT and its various properties.
2. Explain the different Fast–Fourier–Transform (FFT) algorithms along with its applications.
3. Provide the design procedure of IIR filters and FIR filters using different techniques.
4. Provide the design of IIR filters from analog filters using different methods.
5. Provide implementation scheme of IIR and FIR filters using different methods.
6. Provide exposure to different applications of DSP.

UNIT – I	**8 Hours**

Discrete Fourier Transforms (DFT): Frequency Domain Sampling and Reconstruction of discrete-time Signals, Discrete Fourier Transforms, DFT as a linear transformation, its relationship with other transforms. Properties of DFT– Periodicity, linearity and Symmetry Properties, Multiplication of two DFTs–the circular convolution, use of DFT in linear filtering, overlap–save and overlap–add method.
Text1:7.1.1 ,7.1.2, 7.1.3, 7.1.4, 7.2.1 7.2.2, 7.2.3, 7.3.1

Self-study component:	Additional properties of DFT (circular-time shift, Circular- frequency shift, Time reversal, circular convolution, parseval's relation).
Practical Topics:	1. Develop MAT Lab code for Computation of the N point DFT and IDFT of a given sequence and to plot magnitude and phase spectrum. 2. Develop MAT Lab code Circular convolution of the two given sequences without using function and using DFT and IDFT. 3. Develop MAT Lab code for Linear convolution using DFT and IDFT without using inbuilt function and simulate.

UNIT – II	**8 Hours**

Fast–Fourier–Transform (FFT) Algorithms: Efficient computation of the DFT (FFT algorithms), Direct computation of DFT, Goertzel algorithm, and chirp–z transform. Radix–2 FFT algorithm for the computation of DFT and IDFT–decimation in–time and decimation–in –frequency algorithms.
Text1: 8.1, 8.1.1, 8.1.2, 8.1.3, 8.1.5, 8.1.6, 8.2

Self-study component:	Applications of FFT algorithm. (Using MATLAB or SCILAB or any similar tools)
Practical Topics:	1. Develop MAT Lab code for Computing the frequency spectrum of a given sequence using FFT and IFFT. 2. Develop MAT Lab code for Autocorrelation andCross correlation of the given sequence and verification of its properties. 3. Develop MAT Lab code for voice and Music. Plot the spectrum.

UNIT – III	8 Hours
FIR Filter Design: Characteristics of Practical Frequency Selective filters, FIR filter design: Introduction to FIR filters, design of FIR filters using – Rectangular and Hamming windows, FIR filter design using frequency sampling technique **Text1:** 10.1.2, 10.2.1, 10.2.2, 10.2.3, 10.4	
Self-study component:	Hanning window, Blackmann window
Practical Topics:	1. Design and Develop MAT Lab code for FIR Filters to meet the given specifications using Simulink. 2. Experiments Using Digital Signal Processor (TMS320c54xx) And Code Composer Studio (CCS) a. Circular convolution of the two given sequences.

UNIT – IV	8 Hours
Design of IIR Filters From Analog Filters (Butterworth and Chebyshev) : Characteristics of commonly used analog filters – Butterworth and Chebyshev filters., analog to analog frequency transformations. Impulse invariance method. Mapping of transfer functions: Approximation of derivative (backward difference and bilinear transformation) method. **Text1:** 10.3.1, 10.3.2, 10.3.3 ,10.3.4,10.4.1	
Self-study component:	1. Matched z transforms 2. Transform the analog filter H(S)=$\frac{S+3}{(S+1)(S+2)}$ to a digital filter using Matched Z-Transform(T=0.5sec).
Practical Topics:	1. Design and develop MATLab code for IIR Filters to meet the given specifications using Simulink. 2. Experiment Using Digital Signal Processor (TMS320C54xx) and Code Composer Studio (CCS): Computation of the N Point DFT of a given sequence.

UNIT – V	8 Hours
Implementation of Discrete–Time Systems: Structures for IIR and FIR systems– direct form I and direct form II systems, cascade and parallel realization, Applications of DSP **Text1:** 9.1, 9.2, 9.3 **Text 2:** 12.1 to 12.8	
Self-study component:	Speech processing.
Practical Topics:	1. Analyze the impulse response and step response of a system using MATLAB/SIMULINK 2. Analyze the operation of Basic Communication model using Simulink. 3. Noise: Add noise above 3 kHz and then remove; Interference suppression using 400 Hz tone.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Explain and solve the** DFT, FFT and Filters problems.	Understand and Apply	PO1(L3)

CO2	**Differentiate the** DFT, FFT,IDFT,IFFT and filtering techniques.	Analyze	PO1(L1),PO2(L3)
CO3	**Appraise** the discrete–time systems using various DSP approaches	Evaluate	PO2(L2),PO3(L4)
CO4	**Design** the FIR & IIR filters for given specification	Create	PO2(L2),PO3(L5)
CO5	**Conduct** experiments to **verify** DSP concepts and applications of DSP using **Hardware DSP board**.	Create	PO3(L3),PO5(L3),PO9(L2)

Text Book(s):

1. **"Digital Signal Processing – Principles Algorithms and Applications",**Proakis&Monalakis,PHI / Pearson Education, 4th Edition, New Delhi,2007.ISBN:978-81-317-1000-5
2. **"Digital signal Processing"**–A.NagoorKani,McGraw hill education,2nd edition,NewDelhi 2012.ISBN-13: 978-0-07-008665-4, ISBN-10: 0-07-008665-6.

Reference Book(s):

1. **"Discrete Time Signal Processing"**, Oppenheim and Schaffer, PHI,2003, ISBN - 10:9332535035, ISBN-13:9789332535039.
2. **"Digital Signal Processing",** S. K. Mitra, Tata Mc–Graw Hill, 3rd Edition, 2007.ISBN: 9780070667563, ISBN-007066756X.
3. **"Digital Signal Processing",** Lee Tan, Elsevier publications, 2007.ISBN-9780124159822, ISBN-9780124158931.
4. **"Digital Signal Processing using MATLAB",**Sanjit K Mitra, TMH, 2001
5. **"Digital Signal Processing using MATLAB**", J.G. Proakis& Ingle, MGH, 2000

Web and Video link(s):

http://acl.digimat.in/nptel/courses/video/117102060/L01.html

E-Books/Resources:

1. http://libgen.rs/book/index.php?md5=8FA146CE83BC35BE9171560760124653
2.http://libgen.rs/book/index.php?md5=D4D60EB785E913243C06C021246C2EE4

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2	2	3											2	3
#3		2	3											2
#4		2	3											2
#5			3		3				2					

Open Elective –I
E-Waste Management
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – V

Course Code:	**P21EC5051**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives:

1. Understand importance of Electrical and Electronics waste management
2. Awareness about global rules and standards with respect to E-waste management
3. Acquire knowledge of materials used in E & E products and their disposition
4. Knowledge of Recycling and Recovery technologies.
5. Analysis of typical electronic devices their constituents and recyclability.
6. To understand OEM and allied vendor responsibility towards recyclable products and Manufacturing standards.

UNIT – I **8 Hours**

Introduction and Overview: Introduction, WEEE–The Scale of the Problem, Legislative Influences on Electronics, Recycling, Producer Responsibility Legislation, The WEEE Directive, The RoHS Directive, Other Examples of Legislation, Treatment Options for WEEE, Material Composition of WEEE, Socio-economic Factors, Logistics of WEEE, Barriers to Recycling of WEEE, the Recycling Hierarchy and Markets for Recyclate, WEEE Health and Safety Implications.
Text1: PageNo:1 to 17, 24 to 35

Self-study component:	Prepare a statistical survey report on Indian scenario of electronic sales and purchase.

UNIT – II **8 Hours**

Materials Used in Manufacturing Electrical and Electronic Products: Perspective, Impact of Legislation on Materials Used in Electronics, Overview, The RoHS Directive and Prescribed Materials, Where do RoHS Prescribed Materials Occur?, Lead, Brominated Flame Retardants, Cadmium, Mercury and Hexavalent Chromium, Soldering and the Move to Lead-free Assembly, Lead-free Solder Choices, Printed Circuit Board Materials, PCB Materials, Provision of Flame Retardancy in PCBs, Non-ferrous and Precious Metals, Encapsulants of Electronic Components, Indium Tin Oxide and LCD Screens, Polymeric Materials in Enclosures, Casings and Panels, Product-related Plastic Content, WEEE Engineering Thermoplastics, Polycarbonate (PC), ABS (A crylonitrile-Butadiene-Styrene), High Impact Polystyrene (HIPS), Poly phenylene oxide (PPO), PC/ABS Blends, Flame Retardants in Engineering Thermoplastics, Materials Composition of WEEE, Mobile Phones, Televisions, Washing Machines.
Text 1: PageNo:40 to 73

Self-study component:	Present a short summary on European Commission's 1991 Battery Directive (91/157/EEC) and its implications

UNIT – III **8 Hours**

Part-I Recycling and Recovery: Introduction, Separation and Sorting, Treatment, Mixed WEEE, Refrigeration Equipment, Cathode Ray Tubes, Individual Processes, Outputs and Markets, Metals, Glass, Plastics, Emerging Technologies, Separation, Thermal Treatments, Hydrometallurgical Extraction, Sensing Technologies, Plastics to Liquid Fuel, Plastics Containing Brominated Flame Retardents.
Part-II Integrated Approach to e-Waste Recycling: Introduction, Recycling and Recovery Technologies, Sorting/Disassembly, Crushing/Diminution, Separation, Emerging Recycling and

Recovery Technologies, Automated Disassembly, Commintion, Separation, Thermal Treatments, Hydrometallurgical Extraction, Dry Capture Technologies, Biotechnological Capture, Sensing Technologies, Design for Recycling and Inverse, Manufacturing **Text 1: PageNo:91 to 107,111 to 120**	
Self-study component:	Present a report on e-waste management and recycling initiatives of companies like: SONY, Philips and Samsung etc.

UNIT – IV	**8 Hours**
Sector-based Eco-design, Disassembly, Fasteners, RFIDs (Radio Frequency Identification Tags), Active Disassembly, Design Methodology and Resource Efficiency, Recycling, Constraints on Materials Selection, Eco-design Guidelines for Manufacturing.(Ch5. Pg.N0.141-160), Liquid Crystal Displays: from Devices to Recycling: Overview of Liquid Crystals Definition and Classification of Liquid Crystals, Molecular and Chemical Architecture of Liquid Crystals, The **Mesosphere:** Types of Intermediate State of Matter, Physical Properties of Liquid Crystals and Material Requirements, Overview of Liquid Crystal Displays Based on Nematic Mesophase, Basic LCD Operating Principles, Types of Electro-optic LCD Devices, LCD Manufacturing Process, Environmental Legislation and Lifecycle Analysis. The WEEE Directive and LCDs, RoHS and REACH, Far East Environmental Measures, Lifecycle Analysis, Potentially Hazardous Constituents: Toxicity of LCD Constituents, Toxicity of Mercury and Backlighting, Toxicity of Liquid-crystal Mixture, Demanufacture and Recycling. **Text 1: PageNo:180-204**	
Self-study component:	Refer the websites: 1. https://www.epa.gov/, 2. https://sustainabilityguide.eu Understand the significance of design for sustainability.

UNIT – V	**8 Hours**
The Role of Collective versus Individual Producer Responsibility in e-Waste Management: Key Learning's from Around the World: Brief Introduction to WEEE, The WEEE Directive, Producer Responsibility, Household and Non-household WEEE, E-waste and Its Environmental Impacts, Marking EEE Products, WEEE Collection Points, Product Categories and Waste Streams, Producer Compliance Schemes, Variations in National WEEE Laws, Background to Producer Responsibility, Defining Individual and Collective Producer, Responsibility, The WEEE Directive in Europe, The WEEE Directive's Approach to Individual and Collective Producer Responsibility, Implementation of Individual and Collective Producer Responsibility in the EU, ICT Milieu, The Netherlands, E-waste Laws and Voluntary Agreements in Other Countries, Japanese Electronics Take-back Directive, Product Take-back in the USA, Product Stewardship in Australia. **Text 1: PageNo:161 to 164, 212 to 222**	
Self-study component:	Write a short note on "A model for optimal product recovery in the context of Extended Producer Responsibility".

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO#) with BTL**
CO1	**Apply** the knowledge of basic sciences to understand the issues of Electrical and Electronic Equipment Wastes and societal responsibility**.**		PO1, PO7[L3]

CO2	**Analysis** of material used in current EEE and legislative directives.		PO2, [L3]
CO3	**Knowledge** of WEEE Directives, RoHS Directives, Health hazards, Recycling, Recovery technologies and future technologies.		PO1, [L4]
CO4	**Analyze t**ypical electronic ++devices and PCBs their constituent hazards, recyclability and treatment technologies.		PO2, [L3]
CO5	**Understand** need of waste management OEM and allied vendor responsibility to wards recyclable products and Manufacturing standards and nation wise initiatives.		PO2,PO7 [L2]

Text Book(s):

1. **"Electronic Waste Management**" edited by Ronald E. Hester, Roy M. Harrison, RSC Publishing. ISBN: 9780854041121**.**

Reference Book(s):

1. **"E-Waste: Management, Types& Challenges (Computer Science, Technology andApplications: Environmental Remediation Technologies, Regulations and Safety)".**YuanChun Li, BanciLian Wang, Nova Science Publishers, 2012, ISBN: 1619422174.
2. "**Electronic Waste: High-Impact Strategies - What You Need to Know: Definitions, Adoptions, Impact, Benefits, Maturity, Vendors, Kevin Roebuck",**Emereo Publishing, 2011.ISBN: 9781743339084.

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3						1						3	
#2		3												3
#3	2												2	
#4		2												2
#5		2					2							2

Principles of Communication Systems [As per Choice Based Credit System (CBCS) & OBE Scheme] **SEMESTER – V**			
Course Code:	**P21EC5052**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives (CLOs):This course aims to:

1. Provide the basic knowledge on Electronic Communication Systems.
2. Describe the concept of Amplitude Modulation and Frequency modulation.
3. Explore the concept of Digital Communication Systems.
4. Explain the concept and importance of Satellite communication.
5. Understand the Fundamentals of Networking and Local Area Network
6. Describe the importance and applications of Cell phones

UNIT – I	**8 Hours**

Introduction to Electronic Communication: The significance of human communication, Communication Systems, Types of Electronic Communication, Modulation and Multiplexing, The Electromagnetic Spectrum, Bandwidth

Amplitude Modulation Fundamentals: AM Concepts, Modulation Index and Percentage of Modulation, Sidebands and the Frequency Domain, AM Power,

Text 1:1.1-1.6, 3.1-3.4

Self-study component:	Amplitude Demodulators, Diode Detectors, Crystal Radio Receivers, Synchronous Detection.

UNIT – II	**8 Hours**

Fundamental of Frequency Modulation: Basic Principles of Frequency Modulation, Modulation index and side bands, Frequency modulation Versus Amplitude Modulation.

Digital Communication Techniques: Basic Principles of Signal Reproduction, Super heterodyne receivers.

Text 1: 5.1, 5.3, 5.5, 9.1,9.2

Self-study component:	Principles of Phase Modulation, Digital transmission of data.

UNIT – III	**8 Hours**

Multiplexing and DE multiplexing: Multiplexing Principles, Frequency division Multiplexing, Time-Division Multiplexing, Pulse-code Modulation, Duplexing

Fundamentals of Networking and Local Area Networks: Network Fundamentals**,** LAN hardware.

Text 1: 10.1-10.5, 12.1-12.2

Self-study component:	Ethernet LANs - Topology, Encoding, Speed, Transmission Medium, and Advanced Ethernet.

UNIT – IV	**8 Hours**

Satellite Communication: Satellite Orbits, Satellite communication systems, Satellite Subsystems, Ground Stations, Satellite Applications,

Text 1:17.1-17.5.

Self-study component:	Make a study of advances made by India in Satellite communication, Global Navigation System.

UNIT – V	8 Hours

Cell Phone Technologies: Cellular Telephone Systems, A Cellular Industry Overview, 2G and 3G Digital Cell Phone Systems, Long Term Evolution and 4G Cellular Systems, Base Stations and small cells.

Text 1: 20.1-20.5.

Self-study component:	1. WiMAX and Wireless Metropolitan-Area Networks. 2. Case study: To improve the quality of service in communication (Ref: Zayan EL Khaled and Hamid Mcheick, Case studies of communications systems during harsh environments: A review of approaches, weaknesses, and limitations to improve quality of service, International Journal of Distributed Sensor Networks 2019, Vol. 15(2))

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	**Apply** the basic knowledge Electronic and Communication to distinguish between analog and digital communication systems.	**Understand and Apply**	**PO1,L2**
CO2	Comprehend the concept of Networking and modulation techniques.	**Apply**	**PO1,L2**
CO3	**Illustrate** the conceptual understanding of satellite and wireless communications.	**Apply**	**PO1,L2**
CO4	**Analyze** at block level the use of various Communication Techniques.	**Analyze**	**PO1,PO2,L2,L3**
CO5	**Articulate** the working of Cell Phone Technologies, multiplexing and de multiplexing in electronic communication systems.	**Apply and Analyze**	**PO1,PO2,L2**

Text Book(s):

1. **"Principles of Electronics Communication System",** Louis E FrenzelJr, 4th edition. ISBN 978-0-07-337385-0, Mcgraw Hill Publication

Reference Book(s):

1. **"Digital Communication",** P. Ramakrishna Rao, TATA McGraw Hill,2011, ISBN:9780070707764.
2. **"Wireless and Mobile Communication"** by Sanjeev Kumar, New age International Publishers- 2010 Edition, ISBN(10):81-224-2354-X, ISBN(13):978-81-224-2354-9
3. **"Mobile Cellular Telecommunication",** Lee W.C.Y, McGraw Hill, 2002, ISBN: 9780071436861, 0071436863
4. **"Satellite Communications",** Dennis Roddy, 4th Edition, Special Indian Edition 2009, 11th reprint 2013 McGraw–Hill, ISBN13:978-0-07-007785-0, ISBN 10:0-07-007785-1

Web and Video link(s):

1.https://onlinecourses.nptel.ac.in/noc22_ee05/preview
2.https://archive.nptel.ac.in/courses/108/104/108104091/

E-Books/Resources:
https://physicaeducator.files.wordpress.com/2018/03/principles-of-electronic-communication-system-by-luies.pdf

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2	3												3	
#3	3												3	
#4	2	2											2	2
#5	3	2											3	2

Biometrics
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – V

Course Code:	**P21EC5053**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course aims to:

- Provide the basic knowledge on biometrics and its modality.
- Analyze the hand written character recognition system.
- Describe the concept of different physical biometrics.
- Interpret biometric hand gesture recognition for Indian sign language.
- Discover the privacy issues and concerns related to biometrics.
- Discuss bio metriccryp to graphy and multimodal biometrics.
- Explain the importance of watermarking techniques in biometrics.
- Summarize the scope and future of biometrics and its standards.

UNIT – I **8 Hours**

Introduction: What is Biometrics? History of biometrics**,** Types of biometric traits**,** General architecture of biometric system, Basic working of biometric matching (Templates)**,** Biometric system error and performance measures, Design of biometric systems**,** Applications of biometrics, Benefits of biometrics versus Traditional authentication methods.

Handwritten Character Recognition: Introduction**,** Character recognition**,** System overview**,** Feature extraction for character recognition**,** Neural network for hand written Character recognition, Multilayer neural network for hand written character rrecognition**.**

Text1: 1.1-1.9 and 2.1-2.6

Self-study component:	1. Devanagarinumeral recognition 2. Isolatedhandwrittendevanagaricharacterrecognitionusingfourierdescriptorandhidden**.**

UNIT – II **8 Hours**

Face Biometrics: Introduction**,** Background of face recognition**,** Design of face recognitionsystem**,** Neural network for face recognition**,** Face detection in video sequences**,** Challenges infacebiometrics**,** Facerecognitionmethods**,** Advantagesanddisadvantages.

RetinaandIrisBiometrics: Introduction**,**Performanceofbiometrics**,**Designofretinabiometrics, Design of iris recognition system**,** Iris segmentation method**,** Determination of irisregion**,** Applications of iris biometrics**,** Advantages anddisadvantages.

Text1:3.1-3.8, 4.1-4.6, 4.8, 4.9

Self-study component:	1. Face Recognition Smart Attendance System (Reference Paper: Alhanaee, K., Alhammadi, M., Almenhali, N., &Shatnawi, M. (2021). Face recognition smart attendance system using deep transfer learning. Procedia Computer Science, 192, 4093-4102.) 2. List the challenges in capturing retina and iris information.

UNIT – III **8 Hours**

Vein and Fingerprint Biometrics: Introduction**,** Biometrics using vein pattern of palm**,** Fingerprint biometrics, Finger printer cognition system, Minutiae extraction**,** Finger print indexing**,** Advantages and disadvantages.

Biometric Hand Gesture Recognition for Indian Sign Language: Introduction**,** Basics of hand geometry**,** Sign language, Indian sign language (ISL), SIFT algorithm, Advantages and disadvantages.

Text1:5.1- 5.6, 5.8and6.1-6.5, 6.7.

Self-study component:	1. Study different practical hand gesture recognition techniques. 2. Study Fingerprint Minutiae Extraction and Matching based on SIFT Features. (Reference Paper: Bakheet, S., Alsubai, S., Alqahtani, A., &Binbusayyis, A. (2022). Robust Fingerprint Minutiae Extraction and Matching Based on Improved SIFT Features. Applied Sciences, 12(12), 6122.)

UNIT – IV	**8 Hours**

PrivacyEnhancementUsingBiometrics: Introduction**,**Privacyconcernsassociatedwithbiometricdeployments,Identityandprivacy,Privacyconcerns,Biometricswithprivacyenhancement**,**Comparisonofvariousbiometricsintermsofprivacy,SoftBiometrics.

BiometricCryptographyandMultimodalBiometrics: Introductiontobiometriccryptography, General purpose cryptosystem, Modern cryptography and attacks, Symmetric keyciphers, Cryptographic algorithms, Introduction to multimodal biometrics, Basic architecture ofmultimodalbiometrics,Multimodalbiometricsusingfaceandear,Characteristicsandadvantagesofmultimodalbiometrics.

Text1:7.1-7.7 and 8.1-8.9

Self-study component:	1. AADHAAR: Anapplication of multimodal biometrics. 2. Study the security of biometric data using cryptography. (Reference Paper: Thawre, A., Hariyale, A., &Chandavarkar, B. R. (2021, May). Survey on security of biometric data using cryptography. In 2021 2nd International Conference on Secure Cyber Computing and Communications (ICSCCC) (pp. 90-95). IEEE.)

UNIT – V	**8 Hours**

WatermarkingTechniques: Introduction,Datahidingmethods**,**Basicframeworkofwatermarking**,**Classificationofwatermarking**,**Applicationsofwatermarking**,**Attacksonwatermarks,Performanceevaluation**,**Characteristicsofwatermarks,Generalwatermarkingprocess**,**Imagewatermarkingtechniques**,** Watermarking algorithm.

Biometrics Scope and Future: Scope and future market of biometrics, Biometric technologies**,** Applications of biometrics**,** Biometrics and information technology infrastructure**,** Role of biometrics in enterprise security**,** Role of biometrics in border security**,** Smart card technologyandbiometrics**,**Radiofrequencyidentification(RFID)biometrics,DNAbiometrics**,**Comparativestudyofvariousbiometrictechniques.

Biometric Standards: Introduction, Standard development Organizations, Application Programming Interface (API), Information Security and Biometric Standards, Biometric Template Interoperability.

Text1: 9.1- 9.11, 10.1-10.10 and 12.1-12.5.

Self-study component:	1. Understand the concepts of Digital Image Watermarking (Reference Paper: Wadhera, S., Kamra, D., Rajpal, A., Jain, A., & Jain, V. (2022). A comprehensive review on digital image watermarking. arXiv preprint arXiv:2207.06909. 2. List the scope of biometric devices in future security systems.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Explain** the basics of biometric modalities and features of the biometrics.	Analyze	PO2(L3)

CO2	**Apply** the various morphological operations for feature extraction in various biometrics.	Apply	PO1(L3)
CO3	**Analyze** the use of various biometrics.	Analyze	PO2(L3)
CO4	**Understand** the role of watermarking techniques in biometrics.	Understand and Apply	PO1(L2)

Text Book(s):

1. **"Biometrics: Conceptsan Applications"**,G.R.Sinha,SandeepB.Patil,Wiley,2013edition. ISBN:13:978-81-265-3865-2.

Reference Book(s):

1. Samir Nanavati, Michael Thieme, Raj Nanavati, **"Biometrics – Identity Verification ina Networked World"**, Wiley-dreamtech India Pvt Ltd, New Delhi, 2003. .ISBN: 978-0-471-09945-1
2. PaulReid,**"BiometricsforNetworkSecurity"**,PearsonEducation,NewDelhi,2004.ISBN10:81 31716007.
3. JohnRVacca,**"BiometricTechnologiesandVerificationSystems"**,ElsevierInc,2007.ISBN:978 0750679671.
4. AnilKJain,PatrickFlynn,ArunARoss,**"Handbook ofBiometrics"**, Springer,2008.ISBN978-0-387-71041-9

Web and Video link(s):

1. https://www.digimat.in/nptel/courses/video/106104119/L22.html
2. https://www.youtube.com/watch?v=GMDggxifxqk

E-Books/Resources:

1. http://libgen.rs/book/index.php?md5=BD06463CF54045664E21537332BA95D4
2. http://libgen.rs/book/index.php?md5=57E403ABF891F363697612ED3B61161F
3. http://libgen.rs/book/index.php?md5=CB08E0F34881899E31B034753DD6D831
4. http://libgen.rs/book/index.php?md5=20A2D412E15640F3E50D132E8216BA39
5. http://libgen.rs/book/index.php?md5=F23D36C457D852BBD206E694400A2ACD

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1		3												3
#2	3												3	
#3		3												3
#4	2												2	

Sensors and IOT

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – V

Course Code:	**P21EC5054**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. To understand the fundamentals of IOT.
2. To learn about the basics of IOT Protocol.
3. Illustrate Mechanism and Key Technologies in IOT.
4. To develop IOT applications using Raspberry Pi and apply Cloud services for IOT systems.
5. To learn about the fundamentals of sensors.

UNIT – I **8 Hours**

Introduction to Internet of Things: Definition and Characteristics of IoT, Physical Design of IoT, IoT Protocols, IoT communication models, IoT Communication APIs, IoT enabled Technologies, Wireless Sensor Networks, Cloud Computing, Big data analytics, Communication protocols, Embedded Systems, IoT Levels and Templates.

Domain Specific IoTs: Introduction, Home Automation, Cities, Environment, Energy, Retail.

Text 1: 1.1 to 1.5 and 2.1 to 2.5

Self-study component:	Inventory management, logistics, Agriculture

UNIT – II **8 Hours**

Internet of Thing and Machine-to-Machine: Introduction, M2M, Difference between IoT and M2M, Software Defined Radio (SDR) and Network Function Virtualization (NFV).

IoT Systems – Logical Design using Python: Introduction, Python data types and data structures, Control flow, Functions, Modules, Packages, File handling, Date/Time Operations, Classes.

Text 1: 3.1 to 3.4.1 and 6.3 to 6.10

Self-study component:	Need for IoT management systems, IoT management systems

UNIT – III **8 Hours**

IoT Physical Devices and Endpoints: What is an IOT device, Raspberry Pi, About the board, Linux on Raspberry Pi, Raspberry Pi interfaces, Programming Raspberry Pi with Python.

IOT Physical Servers and Cloud Offerings: Introduction to Cloud storage models and communication APIS, WAMP-AutoBahn for IOT, Xively Cloud for IOT, Python Web –Application Framework-Django.

Text 1: 7.1 to 7.6 and 8.1 to 8.4

Self-study component:	1. Understand the concept of python packages of interest for IoT using Java Script Object Notation (JSON). Develop a python code parsing XML file (both creating and parsing). 2. Understand the need of different IoT devices used to implement an embedded application.

UNIT – IV **8 Hours**

Introduction: Definition of Sensor and Actuator, The Domain of Physical Phenomena, Classification of Sensors and Actuators, Regarding the Energy Source, Regarding the Signal Conditioning, Regarding the Reference Value, Regarding the Complexity, Datasheets, Transfer Function, Sensitivity, Range, Accuracy, Precision, Hysteresis, Nonlinearity, Noise, Resolution, Bandwidth, Repeatability, Dead Zone, Saturation.

Micro and Nanotechnology: Introduction, Manufacture, Use of Silicon, Creation of a silicon dioxide layer by thermal oxidation, Chemical Deposition by Vapor, Photolithography, Bulk Micro fabrication, Superficial Micro fabrication, Application Examples.
Text 2: 1.2 to 1.5 and 2.1 to 2.3

Self-study component:	1. The specification of Vishay Semiconductors BPV10NF Photo Diode. 2. The concept of Linear Variable Differential Transformer (LVDT)

UNIT – V	**8 Hours**

Devices Based on the Electric Field: Introduction, Force, Electric Field and Voltage, Concept of Capacity, Capacitive Displacement Sensor, Capacitive Acceleration Sensor, Angular Velocity Sensor (Gyroscope), Capacitive Fingerprint Sensor, Electrostatic Loudspeaker, Electrostatic MEMS Actuator.
Devices Based on Electrical Resistance: Introduction, Definition of Electric Resistance, Potentiometric Displacement Sensors, Dependence of Resistivity with Temperature and Moisture, Resistive Temperature Detector, Thermistor, Integrated Temperature Sensor, Dependence of Resistivity with Deformation, Strain Gauge.
Text 2: 3.1 to 3.9 and 4.1 to 4.9

Self-study component:	1. The Working of Capacitive Accelerometer. 2. The working of Electrostatic Loudspeaker.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	Identify and Understand the requirement of Physical devices to deploy on IoT application which connect to the cloud for real time scenario	Understand and Apply	**PO1 (L3)**
CO2	Analyze the Concept of Cloud and Web services to access/control IoT devices and security of IoT devices	Analyze	**PO1(L2),PO2 (L3)**
CO3	Analyze the essentials and requirement of IoT.	Analyze	**PO1(L2),PO2 (L3)**
CO4	Analyze the requirement of various sensors.	Analyze	**PO2 (L2)**
CO5	Develop a Portable IOT using Raspberry PI	Create	**PO2(L2),PO3 (L3)**

Text Book(s):

1. **"Internet of Things: A Hands-on Approach",** ArshdeepBahga and Vijay Madisetti, Universities Press, 2015, ISBN:978-81-7371-954-7.
2. **"Sensors and Actuators",** Francisco Andre Correa Alegria, World Scientific Publishing Co. Pte. Ltd, ISBN:978-981-124-251-9.

Reference Book(s):

1. **"Designing the Internet of Things"** by Adrian McEwen, Hakim Cassimally, First Edition, Wiley Publishers. ISBN- 9781118430651
2. **"The Internet of Things", Michael Miller,** First Edition, Pearson, 2015. ISBN-13: 978-0-7897-5400-4, ISBN-10: 0-7897-5400-22. "Designing Connected Products", Claire

Web and Video link(s): NPTEL course on "INTRODUCTION TO IOT" by Prof. SudeepMisraIITKharagpur(133)INTRODUCTION TO IOT- PART-I – YouTube
E-Books/Resources: http://libgen.rs/book/index.php?md5=C3B9C7BAFCFF42E0F9B4C3FBE631F16A

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2	2	3											2	3
#3	2	3											2	3
#4		2												2
#5		2	3											2

Circuit Simulation Laboratory [As per Choice Based Credit System (CBCS) & OBE Scheme] **SEMESTER – V**			
Course Code:	**P21ECL506**	**Credits:**	**01**
Teaching Hours/Week (L:T:P):	**0-0-2**	**CIE Marks:**	**50**
Contact Period:	**Lecture :2 Hr, Exam: 2Hr.**	**SEE Marks:**	**50**

This course aims to:

1. Learning computer aided design and simulation tools
2. Design and verification of circuits at system level.
3. Capturing system requirements and optimize design.

Course Content

The design flow must consists of the following

PART –A

Draw the schematic and perform

- Transient analysis using **Pspice simulator** for given specification
  1. Clipper and Clamper Circuit
  2. CMOS Inverter
  3. Current Controlled Voltage Source
  4. Voltage Controlled Current Source
  5. Summing Amplifier

PART –B

For the following set of experiments the design flow must consists of

- Draw the schematic
- Draw the PCB layout and verify with DRC
- Generate the gerber file for given specification

1. Inverting amplifier
2. Design a full adder using basic gates.
3. Monostable / Astablemultivibrator
4. Power supply design with regulators
5. Amplitude modulator

Open ended experiments

1. Temperature monitoring based on environmental condition.
2. Implement home automation with the help of relays.

Course Outcome (CO)

CO #	Course Outcome	Bloom Taxonomy Levels	Program Outcome Addressed (PO #) with BTL
CO1	**Apply** the knowledge of the digital system to design the schematic in PspiceOrcad tools.	Apply and Analyze	**PO1(L3), PO5 (L3)**
CO2	**Interpret** the concept of transient and ac sweep analysis using Pspice Simulator	Analyze	**PO2(L3), PO4 (L4)**
CO3	**Design** PCB for the basic analog and digital circuit using Orcad tool	Apply and Analyze	**PO3(L3), PO5 (L5)**

CO4	**Analyze and Optimize** the circuit for given specification	Create	**PO2(L2), PO3(L2), PO4(L4), PO5(L3)**

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3				3								3	
#2		3		3										3
#3			3		3									
#4		2	2	3	3									2

Internship- II [As per Choice Based Credit System(CBCS) &OBE Scheme] **SEMESTER–IV**			
Course Code:	**P21INT507**	**Credits:**	**01**
Teaching Hours/Week(L:T:P):	**0 : 0 :0**	**CIE Marks:**	**-**
Internship duration:	**2 weeks**	**SEE Marks:**	**100**

All the students registered to II year of BE shall have to undergo a mandatory internship of 02 weeks during the intervening vacation of II and III semesters or III and IV semester. Internship shall include Inter / Intra Institutional activities. A Semester End Examination (Presentation followed by question-answer session) shall be conducted during IV semester and the prescribed credit shall be included in IV semester. The internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequent Semester End Examination after satisfying the internship requirements. (The faculty coordinator or mentor has to monitor the students' internship progress and interact to guide them for the successful completion of the internship.)

List of Activities

1. Activities concerned with the works of Indian scholars like Charaka and Susruta, Aryabhata, Bhaskaracharya, Chanakya, Madhava, Patanjali, Panini and Thiruvalluvar, among numerous others. (Reference NEP 2020, page 04)
2. Activities such as training with higher Institutions or Soft skill training organized by Training and Placement Cell of the respective institutions.
3. Contributionatincubation/innovation/entrepreneurshipcelloftheinstitute.
4. Participation in conferences/workshops/ competitions etc.
5. Learning at Departmental Lab/Tinkering Lab/ Institutional workshop.
6. Andworkingforconsultancy/researchprojectwith-intheinstitute.[Serialnumbers2to6, AICTE Internship Policy.pdf page 8]
7. Learning MS Word, Excel, Microsoft equations, MS drawing tools, MS Power point, etc.
8. Coding.
9. Mini-projects using commercially available assembled electronic products.
10. Debates, quizzes, and group discussions: On technica
11. Essay competitions: Both in Kannada and English on technical topicsal ready studied.
12. Survey and study of published literature on the assigned topic: Technical papersurvey, Preparation of synopsis. Exposure to technical paper publications.
13. Athletics and Sports.
14. Photography.
15. Short film production : Contemporary aspects, Technicalaspects etc.
16. Music Competition (Vocaland Instrumental): Classical–Indian and western, Sugama- Sangeetha (Bhava Geethegalu), Folk songs, film songs etc.
17. Internship in Disaster Management.[AICTEAPH2021-22pdf page166]

18. Solar energy connected activities that help common man. [AICTE APH2021-22 pdfpage166]
19. Working with Smart City Administration.
20. Hackathon (it is a design sprint-like event in which computer programmers and others involved in software development, including graphic designers, interface designers, project managers, and others, often including domain experts, collaborate intensively on software projects).
21. Industrial Safety, Fire Safety, Electrical Safety, Chemical Process Safety, Food Safety etc.
22. Internship and project work in Indian Knowledge System related Areas/Topics.
23. Industrial visits / small scale Industries / Factories / Cottage Industries / substation visit / short project tour, etc., and submission of report.

Documents to be submitted by Students for Internship Evaluation

I. Student's Diary

The main purpose of writing a daily diary is to cultivate the habit of documenting and to encourage the students to search for details. It develops the students' thought process and reasoning abilities. The students shall record in the daily training diary the day to day account of the observations, impressions, information gathered and suggestions given, if any, and activities carried out. It should contain the sketches and drawings related to the observations made by the students. The daily training diary should be signed after every day or at least twice a week by the Faculty/ in charge of the section (external expert) where the student has been working.

The student's Diary should be submitted by the students along with attendance record. It shall be evaluated on the basis of the following criteria:

(i) Regularity in the maintenance of the diary.

(ii) Adequacy and quality of information recorded.

(iii) Drawings, sketches, and data recorded.

(iv) Thought process and recording techniques used.

(v) Organization of the information.

II. Internship Report

After completion of the Internship, the student shall prepare, with daily dairy as a reference, a comprehensive report in consultation with the evaluators to indicate what he has observed and learned in the training period along with the internship outcomes. The training report should be signed by the Evaluator.

The Internship report shall be evaluated on the basis of the following criteria and/or other relevant criteria pertaining to the activity completed.

(i) Originality.

(ii) Adequacy and purposeful write-up.

(iii) Organization, format, drawings, sketches, style, language etc.

(iv) Variety and relevance of learning experience.

Practicalapplicationsrelationshipswithbasictheoryandconceptstaughtinthecourse.

Table–1:IntraandInterInstituteActivitiesandAssessmentRubrics					
Sl No	**Sub Activity Head**	**Performance/ Appraisal**	**Assessment Rubrics (Allotted marks decide the Letter grade)**	**Proposed Document as Evidence**	**Evaluated by**
1	Inter/Intra Institutional Workshop/ Training.	Excellent	80to100	**(i)** Student's Diary and **(ii)** Internship Report along with the certificate issued from relevant authorized Authority	**i)** Institute Faculty together with External Expert if any. **(ii)** Training And Placement Officer. **(iii)** Physical Education Officer or the concerned in charge Officer of the Activity
		Good	79 to 60		
		Satisfactory	59 to 40		
		Unsatisfactory and fail	<39		

Analog CMOS VLSI Design [As per Choice Based Credit System (CBCS) & OBE Scheme] **SEMESTER – VI**			
Course Code:	**P21EC601**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives:

- Describe the basic MOS device physics and models.
- Describe method of the small signal and large signal analysis of amplifiers.
- Understanding the working of single stage MOS amplifiers with analysis.
- Describe the operation of different types of Current mirrors and their applications.
- Analysis and Design of the Operational amplifiers.
- Analysis and design of CMOS oscillators with mathematical model of VCOs.

UNIT – I	**8 Hours**

Single– Stage Amplifiers: MOS Device Models**,** Basic Concepts, Common–Source Stage, Source Follower, Common–Gate Stage, Cascode Stage.
Text 1: 2.4, 3.1to 3.5

Self-study component:	Design and simulate a single stage Amplifier for given requirements across different technologies, note the limitations and benefits.

UNIT – II	**8 Hours**

Differential Amplifiers: Single– Ended and Differential Operation. Basic Differential Pair, Common–Mode Response, Differential Pair with MOS Loads, Gilbert Cell.
Text 1: 4.1 to 4.3, 4.4 to 4.5

Self-study component:	Explore and analyze the Difference Amplifier.

UNIT – III	**8 Hours**

Passive and Active Current Mirrors: Basic Current Mirrors Cascode Current Mirrors, Active Current Mirrors.
Frequency Response of Amplifiers: General Considerations: Explore and analyze the Wilson Current mirror. Miller Effect, Association of Poles with Nodes Common source stage Source Followers.
Text 1: and 5.1 to 5.3 and **6.1-6.3**

Self-study component:	Study and understand the procedure of calculating Network functions along with the analysis of its Poles and Zeros (Ref: Ch.10 of Network Analysis, 3rd edn, M.E. Van Valkenburg, PHI.)

UNIT – IV	**8 Hours**

Frequency Response of Amplifiers: Common Gate stage, Cascode Stage and Differential Pair.
Operational Amplifiers: General considerations, One stage op-amp, Two stage op-amp, Gain Boosting, Comparison, Common Mode feedback,
Text 1: 6.4-6.6, 9.1 to 9.6

Self-study component:	Read and explore the design of Fully differential OPAMP System of Cirrus Logic International (Patent No: US20180062583A1).

UNIT – V	**8 Hours**

Operational Amplifiers: Input Range limitations, Slew rate, Power supply rejection, Noise in Op-amps.
Oscillators: General Considerations, Ring Oscillators, LC Oscillators, Voltage–Controlled Oscillators, Mathematical Model of VCOs.
Text 1: 9.7 to 9.9 14.1 to 14.5

Self-study component:	Read and explore the Qualcomm VCO design.

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	**Use** the knowledge of electronics circuit and circuit theory to understand the MOS devices and analog CMOS circuits	Understand & Apply	**PO1 (L2)**
CO2	**Compare** the different Analog CMOS VLSI circuits(Amplifiers, Op-amps, Oscillators)	Analyze	**PO1(L2),PO2 (L3)**
CO3	**Design** the analog CMOS circuits for the given Specifications.	Create	**PO2(L2),PO3 (L3)**
CO4	**Discuss** the analog CMOS circuits for Different applications.	Create	**PO2(L2),PO3 (L3)**
CO5	**Simulate** the analog CMOS circuits using modern tools.	Create	**PO3(L2),PO5(L2),PO9 (L3)**

Text Book(s):

1. **Design of Analog CMOS Integrated Circuits",** BehzadRazavi, Tata McGraw Hill, Indian Edition, 2008, ISBN:0-07-238032-2.

Reference Book(s):

1. **"CMOS Analog Circuit Design"**, Phillip E. Allen, Douglas R. Holberg, Oxford University Press, 3rd edition 2011, ISBN:9780199765072.
2. **"CMOS Circuit Design, Layout and Simulation"**, R. Jacob Baker, Harry W. Li, David E. Boyce, Prentice Hall of India, 1st edition 2005, ISBN-13:978-0780334168 ISBN-10:0780334167.

ONLINE COURSES AND VIDEO LECTURES:

1. https://nptel.ac.in/courses/117/101/117101105/ (By Prof. A N Chandorkar, IIT, Bombay)
2. https://nptel.ac.in/courses/108/106/108106105/ (By Prof. Aniruddhan S, IIT, Madras) SWAYAM:
3. https://swayam.gov.in/nd1_noc20_ee13/preview (By Prof. HardikJeetendraPandya, IISC, Bengaluru).

D. Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	2												2	
#2	2	3											2	3
#3		2	3											2
#4		2	3											2
#5			2		3				2					

Professional Elective Course – II

ITC and Multimedia Communications

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – VI

Course Code:	**P21EC6021**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Provide the knowledge of probability, information theory and source coding theorem.
- Analyze the efficient data compression methods and describe the most efficient compression method.
- Develop the channel model and channel capacity theorem.
- Describe the linear block codes, cyclic codes and BCH codes.
- Explain the types of multimedia network and its applications.
- Describe the digitization principles of text and images and provide the understanding of digitization techniques of audio.

UNIT – I **8 Hours**

Information Theory and Source Coding: Introduction to Information Theory, Uncertainty and Information, Average Mutual Information and Entropy, Information Measures for Continuous Random Variables, Relative Entropy, Source Coding Theorem, Huffman Coding, Shannon-Fano-Elias Coding, Arithmetic Coding, The Lempel-Ziv Algorithm, Run Length Encoding, Rate Distortion Function, Optimum Quantizer Design, Entropy Rate of a Stochastic Process, Introduction to Image Compression, The JPEG Standard for Lossless Compression, The JPEG Standard for Lossy Compression, Video Compression Standards.

Text 1: 1.1-1.18

Self-study component:	1. Understand the properties of codes and applications of information theory. 2. Study and compare the different lossy and lossless compression.

UNIT – II **8 Hours**

Channel Capacity and Coding: Introduction, Channel Models, Channel Capacity, Channel Coding, Information Capacity Theorem, Parallel Gaussian Channels, The Shannon Limit, and Channel Capacity for MIMO Systems.

Error Control Coding (Channel Coding): Linear Block Codes for Error Correction, Introduction to Error Correcting Codes, basic definitions , Matrix Description of Linear Block, Equivalent Codes, Parity Check Matrix, Decoding of a Linear Block Code, Syndrome Decoding, Error Probability after Coding (Probability of Error Correction), Perfect Codes, Hamming Codes, Low Density Parity Check (LDPC) Codes, Optimal Linear Codes.

Text 1: 2.1-2.8 , 3.1-3.12

Self-study component:	1. Identify the practical Applications of MIMO system. 2. Understand the uses of Linear and non Linear block codes.

UNIT – III **8 Hours**

Cyclic Codes: Introduction to Cyclic Codes, Polynomials, The Division Algorithm for Polynomials, A Method for Generating Cyclic Codes, Matrix Description of Cyclic Codes, Quasi-Cyclic Codes and Shortened Cyclic Codes.

Bose–ChaudhuriHocquenghem (BCH) Codes: Introduction to BCH Codes, Primitive Elements, Minimal Polynomials, Generator Polynomials in Terms of Minimal Polynomials, Some Examples of BCH Codes, Decoding of BCH Codes, Reed-Solomon Codes.

Text 1: 4.1-4.6 , 5.1-5.7

Self-study component:	1. Discuss the concept of Convolutional Codes, AWGN Channel and identify the noises associated. 2. Golay Codes, CRC Codes.

UNIT – IV	**8 Hours**

Multimedia Communications: Introduction, Multimedia information representation, Multimedia networks: Telephone, data, Broadcast television, ISDN and Broadband multiservice digital networks, Multimedia applications: Interpersonal communication, Interactive applications over the internet, Entertainment applications, Application and networking terminology: Media types, Communication modes, Network types.

Text 2: 1.1 to 1.5

Self-study component:	1. Multimedia Electronic mail structure. 2. Multipoint conferencing. 3. Network QoS and Application QoS.

UNIT –V	**8 Hours**

Multimedia Information Representation: Introduction, Digitization principles: Analog signals, Encoder design, and Decoder design, Text: Unformatted text, Formatted text, Hypertext, Images: Graphics, Digitized documents, Digitized pictures, Audio: PCM speech, Video: Broadcast television, Digital Video.

Text 2: 2.1 to 2.5.1, 2.6.1,2.6.2

Self-study component:	1. Digital cameras and scanners. 2. CD-quality audio and Synthesized audio. 3. HDTV formats, PC video and video content.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Level Indicator**
CO1	**Use the** knowledge of mathematics to understand concepts of Probability, Information theory, communication channel and source codes.	Understand & Apply	**PO1 (L3)**
CO2	**Distinguish** different source codes in communication channels.	Analyze	**PO1(L2), PO2(L4)**
CO3	**Design** coding schemes for a given specifications and evaluate for their error correcting capability.	Create	**PO2(L2), PO3(L3)**
CO4	**Compare** different networks and types in Multimedia Communication and its applications.	Analyze	**PO1 (L2),PO2(L3)**
CO5	Simulate different Source codes using modern tool.	Create	**PO3 (L3), PO5(L3), PO9(L3)**

Text Book(s):

1. "**Information Theory, Coding and Cryptography**", Ranjan Bose, 3rd edition. Tata McGraw. ISBN : 978-0-07-0669017, 2016
2. "**Multimedia Communications, Applications, Networks, Protocols and Standards**", Fred Halsall, Fifth Impression, Pearson, 2011.ISBN: 978-81-317-0994-8.

Reference Book(s):

1. **"Digital Communication Systems",** Simon Haykin, John Wiley, 4th edition.ISBN-13: 978-0130426727.
2. **"Error Control Coding",**Shu Lin, Daniel J. Costello, Jr., 2nd Edition, Pearson.
3. "**Multimedia: Computing, Communications and Applications**", Ralf Steinmetz and KlaraNabrsted, Pearson Education, 2004ISBN: 9788177584417.

Web and Video link(s):NPTEL Course links

1. https://nptel.ac.in/courses/108/102/108102117/
2. https://nptel.ac.in/courses/117/105/117105083/#

E-Books/Resources:

1. https://link.springer.com/book/10.1007/978-3-642-20347-3
2. https://link.springer.com/book/10.1007/978-3-319-05290-8

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2	2	3											2	3
#3		2	3											2
#4	2	3											2	3
#5			3		3				3					

Real Time Signal Processing using Simulink [As per Choice Based Credit System (CBCS) & OBE Scheme] SEMESTER – VI			
Course Code:	**P21EC6022**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. Understand and Master over the basics of signal processing using Matlab Simulink tool
2. Apply and implement various filter design in real time applications.
3. Analyze Real Time DSP Using STM32 and its importance.
4. Appreciate Embedded core generation and multi rate signal processing algorithm applications.

UNIT – I	8 Hours

Introduction To MATLAB SIMULINK Tool

Introduction To MATLAB – Explore Various Toolboxes, Creating and Simulating a Model, Modelling Discrete Dynamic Systems, Simulink Solvers- Fixed Step and Variable Step Solvers.
Link: https://fr.mathworks.com/products/simulink.html
Signal Sampling and Quantization: Sampling of Continuous Signal, Signal Reconstruction
Discrete Fourier Transform and Signal Spectrum: Discrete Fourier Transform, Amplitude Spectrum and Power Spectrum, Spectral Estimation Using Window Functions

Text book: 2.1, 2.2 , 4.1, 4.2 4.3

Self-study component:	Zoom FFT

UNIT – II	8 Hours

Finite Impulse Response Filter Design and Application

Finite Impulse Response Filter Format, Fourier Transform Design, Window Method, Realization Structures of Finite Impulse Response Filters, Coefficient Accuracy Effects on Finite Impulse Response Filters
Adaptive Filters and Applications: Introduction to Least Mean Square Adaptive Finite Impulse Response Filters, Basic Wiener Filter Theory and Least Mean Square Algorithm, Applications: Noise Cancellation, System Modeling, and Line Enhancement,

Text book: 7.1, 7.2,7.3,7.7, 7.8, 10.1 10.2 10.3

Self-study component:	Other Application Examples

UNIT – III	8 Hours

Infinite Impulse Response Filter Design

Infinite Impulse Response Filter Format, Bilinear Transformation Design Method, Digital Butterworth and Chebyshev Filter Designs, Higher-Order Infinite Impulse Response Filter Design Using the Cascade Method, Polo-Zero Placement Method for Simple Infinite Impulse Response Filters, Realization Structures of Infinite Impulse Response Filter, Application: 60-Hz Hum Eliminator and Heart Rate Detection Using Electrocardiography

Text book : 8.1, 8.2 ,8.3, 8.4, 8.7, 8.8, 8.9, 8.10

Self-study component:	Coefficient Accuracy Effects on Infinite Impulse Response Filters

UNIT – IV	8 Hours

Multirate DSP

Decimation, Interpolation, Sampling Rate Conversion by Integer and Non-Integer factor,
Multi Stage Implementation, Multirate System Using Frames Concept, Working With Multi-Channel Signals,

Text book1: 12.1-12-4

Self-study component:	Optimising Generator Code	
UNIT – V		**8 Hours**

Embedded Code Generation: Introduction To Embedded Coder,Generating Embedded Code, Data Structures in Generated Code, Embedded Coder Build Process, Integrating Generated Code with External Code, Packaging Generator Code
Link: https://www.mathworks.com/help/ecoder/ug/generating-code-using-embedded-coder.html

Real Time DSP Using STM32:
STM32 Architecture, STM32 Cube Setup And IDE, Build Procedure and Makefile Concepts Communication Protocols (Uart, Spi, I2c), Reading Wav File from Flash and Performing Filtering, Performing Filtering on Live Audio Stream

Link:https://medium.com/@murugansaravanan369/introduction-to-stm32-architecture-b328b4269381,https://www.phippselectronics.com/stm32-cube-ide-tutorial/, https://makefiletutorial.com/, https://www.digikey.in/en/maker/projects/getting-started-with-stm32-how-to-use-spi/09eab3dfe74c4d0391aaaa99b0a8ee17 , https://www.digikey.in/en/maker/projects/getting-started-with-stm32-i2c-example/ba8c2bfef2024654b5dd10012425fa23, https://community.st.com/t5/analog-and-audio/how-to-play-audio-files-using-stm32-part-1/ta-p/49425

Self-study component:	Volume And Mute Applications

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	Explain and comprehend various spectrum analysis and multirate DSP using Simulink tool. .	Understand and Apply	PO1(L3)
CO2	Apply transforms in implementing various embedded code generation.	Analyze	PO1(L1),PO2(L3)
CO3	Analyze and modify the adaptive filtering algorithms for improved performance.	Evaluate	PO2(L2),PO3(L4)
CO4	Design the Filters for given specification in real time signal processing applications	Create	PO2(L2),PO3(L5)
CO5	Develop an interest to study about the real time DSP and designing projects for processing the real time signal for practical applications	Create	PO3(L3),PO5(L3),PO9 (L2)

Text Book(s):
2. Li Tan, Digital Signal Processing - Fundamentals and Applications, 3rd edition.

Reference Book(s):
3. STM32 Arm Programming for Embedded Systems: 14 May 2018 by Shujen Chen (Author), Eshragh Ghaemi (Author), Muhammad Ali Mazidi (Author)
4. Mastering STM32 - Second Edition Author(s) Carmine Noviello

Web and Video link(s):
1 .https://www.mathworks.com/products/simulink.html

E-Books/Resources:
1.https://www.arm.com/-/media/global/resources/education/textbooks/dsp-sample-chapter.pdf?revision=0a9768b9-0a7a-42fe-aba9-

D. Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2	2	3											2	3
#3		2	3											2
#4		2	3											2
#5			3		3				2					

Embedded Systems [As per Choice Based Credit System (CBCS) & OBE Scheme] SEMESTER – VI			
Course Code:	**P21EC6023**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Understand basic components of embedded systems and its characteristic attributes
- Demonstrate the communication interface required to develop an embedded system.
- Analyze embedded design problem and develop system to meet the needs.
- Use of Firmware design tools based the industry requirements.
- Develop a code for the embedded system using Embedded C.
- Choose proper IDE for the design and follow the recent trends in the embedded system design.

UNIT – I	**8 Hours**

Introduction to Embedded Systems: What is an Embedded System, Embedded Systems vs. General Computing Systems, History of Embedded Systems, Classification of Embedded Systems, Major Application Area of Embedded Systems, Purpose of Embedded Systems.
Typical Embedded System: General purpose and domain specific processors, Memory, Sensors and Actuators, Other System Components.
Text 1: 1.1 to 1.6, 2.1.1, 2.2, 2.3, 2.6

Self-Study Component:	1. Discuss 'Smart' running shoes from Adidas- the Innovative Bonding of Lifestyle with Embedded Technology. 2. Demonstration of practical application of embedded design.

UNIT – II	**8 Hours**

Embedded networks: communication interface. Onboard communication interface –I2C, SPI, Serial peripheral interface (SPI), UART. External communication interface- RS -232C and RS-485, USB, Infrared (IrDA), Bluetooth (BT). Need for Device drivers.
Text 1:2.4, 2.4.1.1 to 2.4.1.3 , 2.4.2 , 2.4.2.1 ,2.4.2.2 , 2.4.2.4, 2.4.2.5, 10.9

Self-Study Component:	1. Understand other Communication Interfaces like Controller Area Network (CAN), Wi-Fi etc. 2. Understand different types of Device Drivers

UNIT – III	**8 Hours**

Characteristics and Quality Attributes of Embedded Systems: Characteristics of an embedded system, Quality attributes of embedded systems.
Embedded System- Application and Domain Specific: Consumer (Washing Machine), Automotive.
Hardware Software Co-Design and Program Modeling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language.
Text 1:3.1, 3.2, 4.1, 4.2, 7.1 to 7.3

Self-Study Component:	1. Discuss How to use Or-CAD tool. 2. Understand schematic design using Or-CAD Capture CIS.

UNIT – IV	8 Hours
Embedded Firmware Design and Development: Embedded Firmware Design Approaches Embedded Firmware Development Languages. **Programming in Embedded C:** Programming in Embedded C**,** C vs Embedded C, Compiler vs Cross Compiler, Using C in Embedded C. **Text 1:**9.1 to 9.3, 9.3.1, 9.3.2, 9.3.3.	
Self-Study Component:	1. Understand Embedded C programs to control 8051 microcontrollers. 2. Design and develop any one application as per current industry need using embedded C.
UNIT – V	**8 Hours**
Real-Time Operating System (RTOS) based Embedded System Design: Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking,Task Scheduling, Task Synchronization, how to Choose an RTOS. **Text 1:**10.1 to 10.5, 10.8, 10.10	
Self-Study Component:	1. Analyze Threads, Processes and Scheduling: Putting them all together with programming. 2. Understand different methods of task communication.

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO#) with BTL
CO1	**Apply** the knowledge of Microcontrollers to understand and explain the concepts of Embedded systems.	Apply	PO1 [L2]
CO2	**Analyze** the different issues involved in embedded system development using real time operating systems.	Analyze	PO1,PO2 [L2,L3]
CO3	**Relate** and **Analyze** various communication interfaces involved in designing embedded application	Evaluate, Analyze	PO2, PO3 [L2,L3]
CO4	**Develop** embedded system applications for a given specification using embedded firmware.	Develop, Create	PO3[L3]
CO5	Application of Embedded systems using Modern tools to meet the current industry requirements.	Design, Create	PO3,PO5, PO12 [L2,L3]

Text Book(s):

1. **"Introduction to Embedded Systems",** Shibu K V, Tata McGraw Hill Education Private Limited, 2009,2nd Edition, ISBN (13): 978-0-07-014589-4

Reference Book(s):

1. **"Embedded Systems – A contemporary Design Tool**", James K Peckol, John Weily, 2008.ISBN: 978-1-119-45750-3.
2. **"Embedded Systems Design"**,An Introduction to Processes, Tools, and Techniques by ArnoldS. Berger ISBN:1578200733 CMP Books© 2002

Web and Video link(s):

1. Embedded Systems Design: https://youtu.be/TP1_F3IVjBc
2. Introduction to Real Time Embedded Systems: https://nptel.ac.in/courses/108105057

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2	3	2											3	2
#3		3	2											3
#4			2											
#5			2		2							2		

Operating Systems [As per Choice Based Credit System (CBCS) & OBE Scheme] SEMESTER – VI			
Course Code:	**P21EC6024**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. Provide an Overview of the Operating Systems topics.
2. Examine the issues of Mutual Exclusion and deadlock.
3. Discuss the principal requirements for memory management.
4. Discuss the organization of the I/O functions.
5. Understand the spectrum of computer security attacks.

UNIT – I	**8 Hours**

Operating System Overview: Operating System Objectives and Functions, The Evolution of Operating Systems, Major Achievements, Developments Leading to Modern Operating Systems, Virtual Machines.
Process Description and Control: What Is a Process?, Process States, Process Description, Process Control
Text 1: 2.1-2.5, 3.1-3.4

Self-study component:	Learn the concepts of Multicore Systems. Learn the Execution of the Operating System.

UNIT – II	**8 Hours**

Concurrency: Deadlock and Starvation - Principles of Deadlock, Deadlock Prevention, Deadlock Avoidance, Deadlock Detection, An Integrated Deadlock Strategy, Dining Philosophers Problem.
Text 1: 6.1 - 6.6

Self-study component:	Learn the Concepts of Mutual Exclusion and Semaphore.

UNIT – III	**8 Hours**

Memory Management: Memory Management Requirements, Memory Partitioning, Paging, Segmentation, Security Issues.
Text 1: 7.1 - 7.5

Self-study component:	Comment on Fixed and Dynamic Memory partitioning.

UNIT – IV	**8 Hours**

Uniprocessor Scheduling: Types of Processor Scheduling, Scheduling Algorithms, Traditional UNIX Scheduling
Text 1: 9.1 - 9.3

Self-study component:	Learn about Multiprocessor Scheduling, Real-Time Scheduling.

UNIT – V	**8 Hours**

I/O Management and Disk Scheduling: I/O Devices, Organization of the I/O Function,Operating System Design Issues, I/O Buffering, Disk Scheduling, RAID, Disk Cache.
Text 1: 11.1 - 11.7

Self-study component:	Compare the types of I/O in UNIX, LINUX and WINDOWS.

Course Outcomes: On completion of this course, students are able to:			
COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	Understand the basic structure of operating system	Understand	PO1(L1)
CO2	Interpret the key design areas that have been instrumental in the development of modern operating systems.	Apply	PO1(L3)
CO3	Examine the principal requirements for memory management and I/O management.	Analyze	PO2(L3)
CO4	Distinguish among various types of security threats along with security techniques.	Analyze	PO1(L2),PO2(L3)

Text Book(s):

1. "Operating Systems" by William Stallings, 7e, Pearson India. ISBN-13: 978-9332518803.

Reference Book(s):

1. Operating Systems" by Godbole, 3 edition, McGraw Hill India. ISBN-13: 978-0070702035

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	1												1	
#2	3												3	
#3		3												3
#4	2	3											2	3

Fundamentals of Network Communication [As per Choice Based Credit System (CBCS) & OBE Scheme] **SEMESTER – VI**			
Course Code:	**P21EC6025**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3 : 0 : 0**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

- Understand the evolution of networks and their associated services, and how services are influencing the evolution of modern networks.
- Comprehend the structure, functions, and protocols of the OSI and TCP/IP models.
- Describe/explain the TCP/IP layer functioning, their dependency, and interaction.
- Gain knowledge of Network Interface Cards (NICs) and various types of network cables.
- Learn the principles and mechanisms of routing and routing protocols.
- Explore Wide Area Networks (WANs) and their associated protocols.

UNIT – I	**8 Hours**

Evolution of Communication Networks and their associated services, Computer Network Evolution, Examples of Protocols and Services.

Self-study component:	1. Excercise the Evolution of Computer Communication. 2. Describe HTTP, HTTPS, and SSH Protocols.

UNIT – II	**8 Hours**

Layered Architecture and OSI Model, OSI Unified View of Protocols and Services,
TCP/IP: Architecture and Routing Examples.

Self-study component:	Compare the dependency of the OSI Model and TCP/IP Model in real-time implementation

UNIT – III	**8 Hours**

TCP/IP: TCP/IP Attributes, TCP/IP Architecture, The TCP/IP Protocol Stack, IP Versions
IPv4 Addressing, Subnet Masking, IP Address Registration, Special IP Addresses, and Subnetting.
Network Interface Adapters: NIC Functions, NIC Features, Selecting a NIC, Hardware Resource Requirements.
Text 1:Ch-13, Ch-3.

Self-study component:	Design a network that includes a Hub connecting at least 5 end-user devices and verify its operation.

UNIT – IV	**8 Hours**

Computer Network Devices and Cables: Hubs, Bridges, Routers,Switches, Layer 3 Switches, Coaxial Cable, Twisted Pair Cable, Fiber Optics.
Text 1:Ch-5, Ch-4.

Self-study component:	3. Configure a network with reference to the college network and implement various routing protocols. 4. Configure VLAN to dive the network for the services of Teachers, Students, and Office Staff.

UNIT – V	**8 Hours**

Wide Area Networks: Introduction to Telecommunications, WAN Utilization, Switching Services, Frame Relay.
Text1: **Ch-7**

Self-study component:	1. Configure a WAN network and implement various WAN protocols. 2. Verify the functionality of Frame-relay WAN Protocol.

Course Outcomes: On completion of this course, students are able to:			
COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Explain** the historical development and significance of communication networks and their services.	L2	PO1[L2]
CO2	**Illustrate** the OSI and TCP/IP models, including the functions of each layer.	L2	PO1[L2]
CO3	**Explain** the roles of NICs and different types of network cables used in communication networks.	L2	PO1 [L2]
CO4	**Demonstrate** the functioning and application of various routing protocols in computer network communication.	L2	PO1, PO7 [L2]
CO5	**Analyze** and **characterize** the architecture, protocols, and technologies used in WANs.	L4	PO2 [L4]

Text Book(s):

3. **"Networking The Complete Reference"**, Third Edition, Released March 2015, Publisher(s): McGraw-Hill. ISBN: 9780071827652.

Reference Book(s):

5. "**Computer Networks, A Top-Down Approach**" by Behrouz A. Forouzan and FirouzMosharraf,Tata McGraw-Hill Education, 2011. ISBN 13: 9781259001567.
6. "**Computer Networks**", Andrew S. Tanenbaum, Pearson education, 5e. ISBN-13: 9789332518742.

Web and Video link(s):

4. https://www.coursera.org/learn/fundamentals-network-communications/lecture/d8HQs/evolution-of-communication-networks
5. https://www.coursera.org/lecture/fundamentals-network-communications/layered-architecture-and-osi-model-njImK

E-Books/Resources:

1. https://www.coursera.org/learn/fundamentals-network-communications
2. https://dokumen.tips/documents/networking-the-complete-reference-third-edition-bobbi-sandbergpdf.html?page=9

D. Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2	3												3	
#3	3												3	
#4	2						1						2	
#5		3												3

Professional Elective Course – III
Computer Organization
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – VI

Course Code:	**P21EC6031**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives:

1. ConceptualizethebasicsofOrganizationalissuesofadigitalcomputerandcomparetheperformanceof machine in struction.
2. Expose different ways of communication with I/O Devices.
3. Notice how to perform computer arithmetic operation.
4. Understand working of processing unit using different bus structures.
5. Illustrate different Types of memory devices with their principles.

UNIT – I	**8 Hours**

BASIC STRUCTURE OF COMPUTERS: Basic operational Concepts, Performance.
INSTRUCTION SET ARCHITECTURE: Memory Location and Addresses, Memory Operations, InstructionandInstructionSequencing,AddressingModes,AssemblyLanguage.
Text 1: Ch 1:1.3 to 1.6 Ch 2:2.1-2.5

Self-study component:	Functional Units of Computer, Number representation and Arithmetic Operations, Character representation.

UNIT – II	**8 Hours**

INSTRUCTION SET ARCHITECTURE(Continued):Subroutines, Additional instructions.

BASIC INPUT/OUTPUT: Accessing I/O Devices-I/O Device Interface, Program Controlled I/O, Interrupts-Enabling and Disabling Interrupts, Handling Multiple Devices, Exceptions.

INPUT/OUTPUT ORGANIZATION: BusStructure, Bus Operation-Synchronous Bus, Asynchronous Bus, Arbitration.
Text 1: Ch 2:2.7, 2.8.Ch 3:3.1.1,3.1.2,3.2.1,3.2.2,3.2.6.Ch 7:7.1,7.2.1,7.2.2,7.3.

Self-study component:	Stacks and Interface Circuits.

UNIT – III	**8 Hours**

Memory Management: Memory Management Requirements, Memory Partitioning, Paging, Segmentation, Security Issues.
Text 1: 6.1 - 6.5

Self-study component:	Read Only Memories and Direct Memory Access

UNIT – IV	**8 Hours**

BASIC PROCESSING UNIT: Some Fundamental Concepts, Instruction Execution, Hardware Components, Instruction Fetch and Execution Steps, Control Signals, Hardwired Control
Text 1: Ch 5:5.1 to 5.6.

Self-study component:	CISC Style Processors.

UNIT – V	8 Hours

ARITHMETIC: Multiplication of Signed Numbers, Fast Multiplication-Bit Pair Recoding of Multipliers, Carry-Save Addition of Summands, Integer Division, Introduction to Floating point Numbers and Operations.
Text 1: Ch 9: 9.4, 9.5.1,9.5.2,9.6,9.7.

Self-study component:	Design of Fast Adders and Multiplication of Unsigned numbers.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	Understand the operation and organization of a digital computer system.	Understand	PO1(L1)
CO2	Apply the knowledge of assembly language/ algorithmic techniques to solve the given problem.	Apply	PO1(L3)
CO3	Analyze the given assembly language code snippet.	Analyze	PO1(L2),PO2(L3)
CO4	Design memory modules.	Create	PO3(L3)

Text Book(s):

1. Carl Hamacher, ZvonkoVranesic, SafwatZaky, Computer Organization and Embedded Systems, 6th Edition, Tata McGraw Hill.

Reference Book(s):

1. ComputerOrganization&Architecture,WilliamStallings,9thEdition,PHI,2013.
2. ComputerSystemsDesignandArchitecture,VincentP.Heuring&HarryF.Jordan,2ndEd.Pearsonon Education, 2004.

Web and Video link(s):

1. https://nptel.ac.in/courses/106/103/106103068/
2. https://nptel.ac.in/content/storage2/courses/106103068/pdf/coa.pdf
3. https://nptel.ac.in/courses/106/105/106105163/
4. https://nptel.ac.in/courses/106/106/106106092/
5. https://nptel.ac.in/courses/106/106/106106166/
6. http://www.nptelvideos.in/2012/11/computer-organization.html

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	1												1	
#2	3												3	
#3	2	3											2	3
#4			3											

Digital Image Processing
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – VI

Course Code:	**P21EC6032**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. Understand the fundamentals of digital image processing.
2. Understand the image enhancement techniques used in digital image processing.
3. Understand the image restoration techniques used in digital image processing.
4. Understand the Morphological Operations and Segmentation used in digital image processing.
5. Understand the image Representation and Description in digital image processing.

UNIT – I	**8 Hours**

Digital Image Fundamentals: What is Digital Image Processing?, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception: Structure of the Human Eye, Brightness Adaption and discrimination, Image Sensing and Acquisition, Image Sampling and Quantization.
Text 1: 1.1,1.3-1.5,2.1,2.3,2.4

Self-study component:	1. Comprehend the array versus matrix operations. 2. Origins of Digital Image Processing. 3. Light and the Electromagnetic Spectrum. 4. Representing digital images.

UNIT – II	**8 Hours**

Spatial Domain: The Basics of Intensity Transformation and Spatial Filtering, Some Basic Intensity Transformation Functions: Image Negatives, Log Transformations, Power-Law Transformation. **Smoothing Spatial Filters:** Order-Static Filters, **Sharpening Spatial Filters:** Using The Second derivative for image sharpening-The Laplacian, Using First-Order derivatives for image sharpening-The Gradient.
Filtering in the Frequency Domain: The basic of Filtering in the Frequency Domain: Summary of steps for Filtering in the Frequency domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters.
Text 1: 3.1, 3.2, 3.5, 3.6, 4.7, 4.8

Self-study component:	1. Develop an algorithm to enhance image quality using histogram equalization 2. Histogram Processing 3. Fundamentals of Spatial Filtering.

UNIT – III	**8 Hours**

Restoration:A model of the image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Estimating the Degradation Function, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering.
Text 1: 5.1-5.4, 5.6-5.8.

Self-study component:	1. Develop an algorithm to add various intensity levels of a given noise to an image and remove. 2. Linear Position Invariant Degradations.

UNIT – IV	8 Hours

Color Image Processing: Color Fundamentals, Color Models, Pseudo-color Image Processing: Intensity slicing and color coding.
Morphological Image Processing: Erosion and Dilation, Opening and Closing, the Hit-or-Miss Transforms, Some Basic Morphological Algorithms: Thinning, Thicking.
Text 1: 6.1 - 6.3, 9.2-9.5

Self-study component:	1. Develop an algorithm to extract boundary pixels of an image using morphological operations 2. Boundary Extraction 3. Hole Filling 4. Extraction of Connected components.

UNIT – V	8 Hours

Segmentation: Point, Line, and Edge Detection, Thresholding: Foundation Optium global thresholding using OTSU'S Method, Region Based Segmentation.
Text 1: 10.2, 10.3, 10.4

Self-study component:	1. Define a procedure for estimating the median of an image from its histogram. 2. Threshold the image at the resulting median value and verify that the foreground and background partitions are of approximately equal size.

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	**Implement the** basic mathematical and signal processing knowledge for the different image processing stages.	Understand and Apply	PO1(L1)
CO2	**Differentiate the** images in the spatial/frequency domain using various methods.	**Analyze**	PO2(L2)
CO3	**Distinguish the** image through image segmentation.	**Analyze**	PO2(L2)
CO4	**Use the** knowledge of image processing in Image Restoration, Color, Morphological processing and Representation and Description .	Apply	PO1(L3)
CO5	**Develop** algorithms to perform image processing using modern tool in a group and acquire team playing skills.	Create	PO3(L3),PO5(L3), PO9(L4)

Text Book(s):
1. **"Digital Image Processing",** Rafael C. Gonzalez and Richard E. Woods, Pearson4th Edition 2018, ISBN:9789353062989.

Reference Book(s):
1. **"Digital Image Processing",**S.Jayaraman, S.Esakkirajan, T.Veerakumar, Tata McGraw Hill 2014.
2. **"Fundamentals of Digital Image Processing",** A. K. Jain, Pearson 2004

Web and Video link(s):
1. https://youtu.be/ArKe6zMkXnk
2. https://youtu.be/iZmHHVwp0Ow

E-Books/Resources:

1. https://sde.uoc.ac.in/sites/default/files/sde_videos/Digital%20Image%20Processing%203rd%20ed.%20-%20R.%20Gonzalez,%20R.%20Woods-ilovepdf-compressed.pdf

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2		3												3
#3		3												3
#4	3												3	
#5			3		2				2					

Design for Testability
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – VI

Course Code:	**P21EC6033**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Understand the significance and principles of testability in Integrated Circuits.
2. Identify and categorize the faults in Integrated circuits.
3. Interpret the Test Pattern Generation and related algorithms for Combinational and Sequential Circuits.
4. Analyze the circuits and device test pattern generators for the circuits.
5. Understand the trade-offs associated with designing for testability
6. Articulate the techniques, structure and methods associated with built-in self-test (BIST), boundary scan testing, and fault injection to improve testability

UNIT – I	**8 Hours**

Introduction to Testing: Introduction, Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing.
Fault Modeling: Defects, Errors, and Faults, Functional Versus Structural Testing, Levels of Fault Models, A Glossary of Fault Models, Single Stuck-at Fault.
Text1: 1.1 to 1.4, 4.1 to 4.5.

Self-study component:	Modelling Circuits for Simulation Algorithms for True-Value Simulation

UNIT – II	**8 Hours**

TESTABILITY MEASURES:SCOAP Controllability and Observability, High-Level Testability Measures
Combinational Circuit Test Generation: Algorithms and Representations, Redundancy Identification (RID), Testing as a Global Problem, Definitions, Significant Combinational ATPG Algorithms (Expect Advanced Algorithms).
Text1: 6.1-6.2, 7.1 to 7.5,

Self-study component:	Advanced Test Pattern Algorithms

UNIT – III	**8 Hours**

Sequential Circuit Test Generation: ATPG for Single-Clock Synchronous Circuits, Time-Frame Expansion Method, Simulation-Based Sequential Circuit ATPG.
Memory Test: Memory Density and Defect Trends, Notation, Faults, Memory Test Levels, March Test Notation, Fault Modeling.
Text1: 8.1 to 8.2, 9.1-9.6.2

Self-study component:	Simulation-Based Sequential Circuit ATPG Memory Testing

UNIT – IV	**8 Hours**

Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.
Built-In Self-Test: The Economic Case for BIST, Random Logic BIST.
Text1: 14.1 to14.4,15.1, 15.2.

Self-study component:	Analog and Mixed-Signal Circuit Trends

UNIT – V	**8 Hours**

Built-In Self-Test: Memory BIST, Delay Fault BIST.
Boundary Scan Standard: Motivation, System Configuration with Boundary Scan, Boundary Scan Description Language.
Text 1: 15.3, 15.4, 16.1-16.3.

Self-study component:	Supply current measurement based test (IDDQ TEST) for manufacturing faults in IC's.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	Apply the principles of testability in Integrated Circuits and categorize the faults in Integrated circuits.	Understand and Apply	PO1(L3)
CO2	Interpret the Test Pattern Generation and related algorithms for Combinational and Sequential Circuits.	Analyze	PO1(L2),PO2(L3)
CO3	Analyze the circuits and device test pattern generators for the circuits.	Analyze	PO1(L2),PO2(L4)
CO4	Apply and Analyze the techniques, structure and methods associated with built-in self-test (BIST), boundary scan testing, and fault injection to improve testability	Apply and Analyze	PO1(L2),PO2(L4)

Text Book(s):

1. Michael L. Bushnell, Vishwani D. Agrawal**, "Essentials Of Electronic Testing For Digital, Memory And Mixed-Signal VLSI Circuits"**, KLUWER ACADEMIC PUBLISHERS NEW YORK, BOSTON, DORDRECHT, LONDON, MOSCOW, 2016**,** ISBN13: 978-0-12-408082-9.

Reference Book(s):

1. M. Abramovici, M. A. Breuer and A.D Friedman, "Digital Systems and Testable Design", Jaico Publishing House.
2. P.K. Lala, "Digital Circuits Testing and Testability", Academic Press.

Web and Video link(s):

E-Books/Resources:

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2	2	3											2	3
#3	2	3											2	3
#4	1	3											1	3

Artificial Intelligence and Machine Learning in VLSI
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – VI

Course Code:	**P21EC6034**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will aims to:

1. Understand about Neural Network and Deep Learning
2. Introduce to the concepts of NVDIA GPU, Tensor Processing Unit.
3. Learn streaming graph Theory.
4. Learn In-Memory Computation.
5. Familiarize Near-Memory Architecture.
6. Introduce Machine learning concepts in physical verification and design.
7. Understand statistical analysis using Machine learning.

UNIT – I	**8 Hours**

Introduction: Development History, Development History, Neural Network Classification, , Neural Network Framework.
Deep Learning: Neural Network Layer, Deep Learning Challenges.
Text 1:• Chapter 1 and Chapter 2

Self-study component:	1. Study introduction to AI and ML 2. Write a sample code in python for a neural network application.

UNIT – II	**8 Hours**

Parallel Architecture: Intel Central Processing Unit (CPU), NVIDIA Graphics Processing Unit (GPU), NVIDIA Deep Learning Accelerator (NVDLA), GoogleTensor Processing Unit (TPU). Microsoft Catapult Fabric Accelerator
Streaming Graph Theory: Blaize Graph Streaming Processor, GraphcoreIntelligence Processing Unit
Text 1:• Chapter 3 and Chapter 4

Self-study component:	Study the introduction to NVIDIA GPU applications, Tensor flow.

UNIT – III	**8 Hours**

In-Memory Computation: Neurocube Architecture, Tetris Accelerator, Neuro Stream Accelerator
Near-Memory Architecture: DaDianNao Supercomputer, Cnvlutin Accelerator.
Text 1:• Chapter 6 and Chapter 7

Self-study component:	Study the supercomputer architectures

UNIT – IV	**8 Hours**

Machine Learning in PhysicalVerification, Mask Synthesis, andPhysical Design: Introduction, Machine Learning in Physical Verification, Machine Learning in Physical Design
Machine Learning-Based Aging Analysis: Introduction, Negative Bias Temperature Instability, Related Prior Work, Proposed Technique, Offline Correlation Analysis and Prediction Model, Runtime Stress Monitoring, Results, Conclusions
Text 2:• 4.1, 4.2, 4.4 and Chapter 9

Self-study component:	Study the Machine Learning Applications in VLSI routing.

UNIT – V	8 Hours

Extreme Statistics in Memories: Cell Failure Probability: An Extreme Statistic, Extremes: Tails and maxima

Fast Statistical Analysis Using Machine Learning: Introduction: Logistic Regression-Based Importance Sampling Methodology for Statistical Analysis of Memory Design, Application to State-of-the-Art FinFET SRAM Design

Text 2:• 10.1, 10.2, 10.4, 11.1,11.5

Self-study component:	Study the Machine Learning regression techniques and sampling algorithms.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	Use the mathematical knowledge for understanding the concepts of Neural Network and Deep learning.	Understand and Apply	PO1(L2)
CO2	Select the appropriate architecture for Neutral Network Implementation.	Apply	PO1(L3)
CO3	Analyze the requirement of hardware in Machine Leaning applications.	Analyze	PO2(L3)
CO4	Analyze the verification and physical design problem and Apply AI algorithms to solve the problem.	Analyze	PO1(L2), PO2(L3)
CO5	Analysis and application of AI in Memory Design, Implementation of neural network application using Python.	Create	PO2(L2), PO3(L3),PO5(L2), PO9(L2)

Text Book(s):

1. Albert Chun Chen Liu, Oscar Ming Kin Law, **"Artificial Intelligence Hardware Design: Challenges and Solutions"**, IEEE Press, Wiley, ISBN: 9781119810452
2. Ibrahim(Abe)M.Elfadel,DuaneS.Boning, Xin_Li, **"Machine Learning in VLSI Computer-Aided Design",**Springer, ISBN 978-3-030-04665-1

Reference Book(s):

1. Stuart J. Russell and Peter Norvig ,**"Artificial Intelligence :A Modern Approach"**, *Prentice Hall,4th Edition,1995.*
2. SandeepSaini, KusumLata, and G.R. Sinha, **"VLSI And Hardware Implementations Using Modern Machine Learning Methods"**, CRC Press 2022, ISBN: 978-1-032-06171-9 (hbk) ISBN: 978-1-032-06172-6 (pbk) ISBN: 978-1-003-20103-8 (ebk) DOI: 10.1201/9781003201038

Web and Video link(s):

1. https://www.youtube.com/watch?v=aircAruvnKk
2. https://www.youtube.com/watch?v=aircAruvnKk
3. https://www.youtube.com/watch?v=pMKuULBKxXY

E-Books/Resources:
https://www.google.co.in/books/edition/AI_and_Machine_Learning_for_Coders/gw4CEAAAQBAJ?hl=en&gbpv=1&dq=books+on+ai+and+ml&printsec=frontcover
https://www.google.co.in/books/edition/Machine_Learning_and_Artificial_Intellig/ybyxDwAAQBAJ?hl=en&gbpv=1&dq=books+on+ai+and+ml&printsec=frontcover
https://www.google.co.in/books/edition/Artificial_Intelligence_and_Machine_Lear/lW5_DwAAQBAJ?hl=en&gbpv=1&dq=books+on+ai+and+ml&printsec=frontcover
https://www.google.co.in/books/edition/Deep_Learning/omivDQAAQBAJ?hl=en&gbpv=1&dq=books+on+deep+learning&printsec=frontcover
https://www.google.co.in/books/edition/Neural_Networks_and_Deep_Learning/achqDwAAQBAJ?hl=en&gbpv=1&dq=books+on+deep+learning&printsec=frontcover

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	2												2	
#2	3												3	
#3		3												3
#4	2	3											2	3
#5		2	3		2				2					2

Microwaves and Antennas [As per Choice Based Credit System (CBCS) & OBE Scheme] **SEMESTER – VI**			
Course Code:	**P21EC604**	**Credits:**	**04**
Teaching Hours/Week (L:T:P):	**3:0:2**	**CIE Marks:**	**50**
Total Theory Teaching Hours: **Total Laboratory Hours:**	**40** **24**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. Provide the basic knowledge of Microwave transmission lines, Rectangular waveguides and planar transmission lines.
2. Discuss the working of Microwave active and passive devices.
3. Explain the concepts of types of antenna and parameters of antenna.
4. Discuss the field due to dipole antenna and array of antenna.
5. Describe the structure and working of helical, log-periodic and micro strip antennas and its Design procedure.

UNIT – I	**8 Hours**

Microwave Transmission Lines: Introduction, Transmission lines equations, Characteristic and input impedances, Reflection and transmission coefficients, Standing waves, Planar transmission lines, Strip lines, Rectangular waveguides, TE and TM wave solutions, dominant and degenerate modes.

Text 1: 3.1- 3.5, 3.10, 3.10.1, 3.11 - 3.11.4.

Self-study component:	1. Smith Chart. 2. MIC Manufacturing, Microwave radiation hazards.
Practical Topics: (3 Hours)	1. Measurement of frequency, guide wavelength, power, VSWR and attenuation in a microwave test bench.

UNIT – II	**8 Hours**

Microwave Passive Devices: Attenuators, phase shifters – Precision phase shifter, MIC phase shifter, reciprocal and non-reciprocal phase shifter, Hybrid or magic Tee, Application of Magic –T (excluding E-Plane Tee & H-Plane Tee).

Microwave Solid State Devices: Transferred electron devices (TED) - Gunn diodes, modes of operation, gunn diode oscillator, TRAPATT diodes and Tunnel diodes- equivalent circuit, Tunnel diode Amplifiers, and Tunnel diode oscillator.

Text 1: 6.4.14, 6.4.15, 6.4.16, 10.3-(10.3.1, 10.3.2), 10.4.3, 10.5, 10.5.1, 10.5.2, 10.5.3.

Self-study component:	1. Avalanche transit time devices (ATTD)-IMPATT Diode 2. Directional couplers, Power Dividers and Microstrip Ring Resonator.
Practical Topics: **(9 Hours)**	1. Determination of coupling and isolation characteristics of a micro–strip directional coupler. 2. Measurement of power division and isolation characteristics of a micro–strip 3dB power divider. 3. Measurement of resonance characteristics of a micro– strip ring resonator and determination of dielectric constant of the substrate.

UNIT – III	**8 Hours**

Introduction: Types of Antennas – Wire, Aperture, Micro-strip, Array, Reflector and Lens antennas, Radiation Mechanism – Single wire, Two-Wires and Dipole.

Fundamental Parameters of Antennas: Introduction, Radiation Pattern – Isotropic, Directional, and Omnidirectional Patterns, Principal Patterns, Radiation Pattern Lobes, Field Regions, Radian

And Steradian, Radiation Power Density, Radiation Intensity, Directivity, Gain, Antenna Efficiency, Half-Power Beam width, Beam Efficiency. **Text 2:** 1.1, 1.2, 1.3 –(1.3.1, 1.3.2, 1.3.3), 2.1 to 2.5, 2.7 to 2.10.	
Self-study component:	1. Bandwidth and Radiation efficiency of antenna. 2. Friis Transmission Equation and Radar Range Equation.
Practical Topics: (3Hours)	1. Plot the Radiation pattern and measure the Directivity of Dipole antenna.
UNIT – IV	**8 Hours**
Linear Wire Antennas: Introduction, Infinitesimal Dipole – Radiated Fields, Power density and Radiation resistance, Radian Distance and Sphere, Near-field, Intermediate and Far – field region, Directivity. **Antenna Arrays:** Introduction, Two- Element Array**,** N-Element Linear Array **–** Uniform Amplitude and Spacing-Broadside array, ordinary End fire array and Phased array. **Text 2:** 4.1, 4.2, 6.1, 6.2, 6.3, 6.3.1 to 6.3.3.	
Self-study component:	1. N element linear array: Directivity. 2. Planar Array: Array Factor, Beam width, Directivity.
Practical Topics: (2Hours)	1. Design and Simulate Dipole antenna using Matlab and Plot the Radiation pattern, Directivity and Impedance graph.
UNIT – V	**8 Hours**
Broadband Antennas: Helical Antenna- Design Concepts, Log-periodic Antennas – planar and wire surfaces and dipole array. **Micro strip Antennas:** Introduction- Basic Characteristics, Feeding Methods, Rectangular Patch - Transmission line model. **Text 2:** 10.3, 10.3.1, 11.4, 11.4.1, 11.4.2, 14.1, 14.2, 14.2.1.	
Self-study component:	3. Log periodic dipole array – Design Concepts. 4. Yagi-Uda& circular patch Antenna– Design Concepts.
Practical Topics: **(7 Hours)**	1. Plot the Radiation pattern and measure the Directivity of Micro strip-Rectangular Patch antenna. 2. Design and Simulate Micro strip rectangular patch antenna using Matlab and Plot the Radiation pattern, Directivity and Impedance graph. 5. Measurement of Pitch angle alpha (in degrees), Axial ratio (AR),HPBW (in degrees) and Directivity (dimensionless and in dB)of Helical Antenna using Matlab

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Discuss** the properties of transmission lines, microwave devices, the parameters of antennas and field due to antenna.	Understand and Apply	**PO1**(L2)
CO2	**Interpret** the working and performance of microwave devices, microwave transmission lines, different types of antennas and antenna arrays.	Apply	**PO1**(L3)

CO3	**Examine** the working and performance of microwave transmission lines, devices, antenna and antenna arrays.	Analyze	**PO1(L1), PO2**(L3)
CO4	**Design** the helical ,Log-periodic dipole antenna and microstrip antennas	Create	**PO2(L2), PO3**(L4)

Text Book(s):

1. **"Microwave Engineering",** Annapurna Das, Sisir K Das, 2nd edition-2009, T.M.H, ISBN (13): 978-0-07-066738-9. ISBN (10): 0-07-066738-1.
2. **"Antenna Theory Analysis and Design",** C. A. Balanis, 2nd edition – 2001, John Wiley, ISBN: 9971-51-233-5.

Reference Book(s):

1. **"Microwave engineering",** David M Pozar, 2nd edition – 2004, John Wiley, ISBN: 9780470631553.
2. **"Foundations for Microwave Engineering",** Robert E Collin, 2nd edition – 2009,John Wiley & Sons Inc (Sea) Pte Ltd, ISBN: 9788126515288.
3. **"Microwave Devices and Circuits",** Samuel Y Liao, 3rd edition – 2004, ISBN: 9780135846810.
4. **"Antennas for all Applications",** John D Kraus, Ronald J Marheka, Ahmad s Khan, 3rd edition- 2006, T.M.H, ISBN:9780070601857.

Web and Video link(s):

1. **NPTEL course: "Antennas",** by Prof. Girish Kumar, IIT Bombay. https://nptel.ac.in/noc/courses/noc17/SEM1/noc17-ee03/

E-Books/Resources:

https://www.studocu.com/in/document/dr-ambedkar-institute-of technology/mobile-adhoc-network/annapurna-das-sisir-k-das-microwave-engineering-mc-graw-hill-india-2014/32304541

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	2												2	
#2	3												3	
#3	2	3											2	3
#4		2	3											2

Open Electives – II
Electronic Instrumentation
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – VI

Course Code:	**P21EC6051**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives
This course aims to
1. Discuss the concepts of signal conditioning and data acquisition system
2. Explain the different types of transducers and measurement errors
3. Differentiate between the DC and AC voltmeters
4. Analyze different types of digital voltmeter
5. Analyze the operation of ADC and different types of digital instruments.
6. Describe the operation of instrumentation amplifier and its applications.

UNIT – I	**8 Hours**

Qualities of Measurements: Introduction, Performance Characteristics, Static Characteristics, Error in Measurement, Types of Static Error, Sources of Error, Dynamic Characteristics.
Voltmeters and Multimeters: Introduction, Basic Meter as a DC Voltmeter, DC Voltmeter, Multirange Voltmeter , Extending Voltmeter Ranges, Loading , AC Voltmeter Using Rectifiers, AC Voltmeter Using Half Wave Rectifier, AC Voltmeter Using Full Wave Rectifier, Peak Responding Voltmeter, True RMS Voltmeter.
Text 1: 1.1 to 1.7, 4.1 to 4.6, 4.12 to 4.14, 4.17, 4.18

Self-study component:	List out the companies that manufacture standard voltmeters and ammeters, range of operation and their salient features.

UNIT – II	**8 Hours**

Digital Voltmeters: Introduction, RAMP Technique, Dual Slope Integrating Type DVM, Integrating Type DVM, Most Commonly Used Principles of ADC, Successive Approximations,
Digital Instruments: Introduction, Digital Multimeters, Digital Frequency Meter, Digital Measurement of Time , Universal Counter, Decade Counter, Electronic Counter.
Text 1: 5.1 to 5.6, 5.11, 6.1 – 6.7

Self-study component:	1. List few practical applications of digital Instruments 2. Design a digital meter to measure light intensity(Block diagram approach)

UNIT – III	**8 Hours**

Transducers: Introduction, Electrical Transducer, Selecting a Transducer, Resistive Transducer, Resistive Position Transducer, Strain Gauges, Resistance Thermometer, Thermistor, Inductive Transducer, Differential Output Transducers, Linear Variable Differential Transducer, Piezo Electrical Transducer.
Text 1: 13.1 to 13.11 and 13.15.

Self-study component:	1. List out few electronic and fiber optic sensors which work on the principal of Transducers. 2. Design a weighing machine using single strain gage (Block diagram approach)

UNIT – IV	8 Hours
Signal Conditioning: Introduction, operational amplifier, basic instrumentation amplifier, Applications of instrumentation amplifiers, chopped and modulated DC amplifier. **Recorders:** Introduction, strip chart recorder, galvanometer type recorder, null type recorder, circular chart recorder, X-Y recorder. Text 1: 14.1 to 14.5, 12.1 to 12.6	
Self-study component:	Design an op-amp which amplifies every signal by a factor of 2.5 using any simulator tool ((Multisim, LTspiceetc)
UNIT – V	**8 Hours**
Data Acquisition System (DAS): Introduction, Objective of a DAS, Signal Conditioning of the Inputs, Single Channel Data Acquisition System, Multi-Channel DAS, Computer Based DAS, Digital to Analog and Analog to Digital Converters, Data Loggers, Sensors Based Computer Data Systems. Text 1: 17.1 to 17.9	
Self-study component:	1. Gather information about data acquisition systems and its uses in fiber optic receivers 2. Simulate an ADC and DAC using any simulator (Multisim, LTspiceetc.)

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	Apply the knowledge of basic electrical engineering in understanding basic principles of data acquisition system, measuring systems, transducers, instrumentation amplifier and recorders	**Understand and Apply**	**PO1 (L2)**
CO2	Apply appropriate measuring techniques in measuring electrical and mechanical parameters	**Apply**	**PO1 (L3)**
CO3	Identify and Determine various measuring errors and other measurable parameters in measuring instruments	**Apply**	**PO1 (L3),**
CO4	Analyze the working principle of various electronic measuring instruments.	**Analyze**	**PO2(L3)**
CO5	Design a system for the desired specification in electronic instrumentation.	**Create**	**PO2(L2), PO3 (L3)**

Text Book(s):

1. **"Electronic Instrumentation",** H. S. Kalsi,3rd edition, McGraw Hill, 2010 ISBN: 9780-07-070206-6 ISBN: 0-07-070206-3

Reference Book(s):

1. **"Electronic Instrumentation and Measurements",** David A. Bell, 3rd edition, Oxford University Press, 2015. ISBN:978-0-19-5669614-1
2. **"Modern Electronic Instrumentation and Measuring Techniques",** Cooper, Helfrick, Prentice Hall of India.

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	2												2	
#2	3												3	
#3	3												3	
#4		3												3
#5		2	3											2

Introduction to Embedded Systems [As per Choice Based Credit System (CBCS) & OBE Scheme] SEMESTER – VI			
Course Code:	**P21EC6052**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. Provide the knowledge about basic concepts of embedded systems.
2. Outline the concepts of typical embedded systems and its applications.
3. Describe the characteristics and quality attributes of embedded systems.
4. Provide the knowledge of software hardware co–design and EDLC.
5. Describe the concepts of real time operating system based embedded systems.

UNIT – I	8 Hours

Introduction to Embedded Systems: What is an Embedded system? Embedded System vs. General Computing Systems, History of Embedded Systems, Classification of Embedded Systems, Major Application Areas of Embedded Systems, Purpose of Embedded Systems, Wearable Devices-The Innovative Bonding of Lifestyle with Embedded Technologies.
The Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components.
Text 1: 1.1 to 1.7, 2.1 to 2.6

Self-study component:	1. Study and understand the working operation of the following input devices: (i) IR proximity sensor (ii) Temperature sensor (iii) Humidity sensor. 2. Study the working of Hydraulic and Rotatory Actuators to understand the operation of output devices.

UNIT – II	8 Hours

Characteristics and Quality Attributes of Embedded Systems: Characteristics of an embedded system, Quality attributes of embedded systems.
Embedded Systems- Application and Domain Specific: Washing Machine – Application-Specific Embedded System, Automotive – Domain Specific Examples of Embedded System
Hardware Software Co-Design and Program Modeling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified modeling Language (UML), Hardware Software Trade-offs.
Text 1:3.1, 3.2, 4.1, 4.2, 7.1 to 7.4

Self-study component:	1. List the different areas that UML has been used. 2. Write the state diagram that shows how UML can be used for designing a door system (that can only be opened and closed).

UNIT – III	8 Hours

Real-Time Operating System (RTOS) based Embedded System Design:
Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Task Communication (Excluding Programs), Device Drivers.
Text 1: 10.1 to 10.5, 10.7, 10.9

Self-study component:	1. Understand the basics of Real time operating systems. 2. Implement the multithread application to satisfy i) Two child threads are created with normal priority ii) Thread 1 receives and prints its priority, sleeps for 50 msec and then quits.

UNIT – IV	8 Hours

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages

The Embedded System Development Environment: The Integrated Development Environment(IDE), Types of Files Generated on Cross compilation, Disassembler/ Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

Text 1: 9.1, 9.2, 13.1 (excluding sub articles), 13.2 to13.6

Self-study component:	1. List different IDE tools used for the development of embedded systems with proper examples. 2. Understand the concept of software for Embedded Systems

UNIT – V	8 Hours

The Embedded Product Development Life Cycle (EDLC): What is EDLC, Why EDLC, Objectives of EDLC, Different phases of EDLC, EDLC Approaches.

Trends in the Embedded Industry: Processor Trends in Embedded System, Embedded OS Trends, Development Language Trends, Open Standards, Frameworks and Alliances, Bottlenecks.

Text 1:15.1 to 15.5, 16.1 to 16.5

Self-study component:	1. Discuss the recent key trends used in embedded systems market. 2. Understand the different categories of EDLC.

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	**Apply** the knowledge of Microcontrollers to understand and explain the concepts of Embedded systems.	Understand and Apply	PO1 (L2)
CO2	**Analyze** the different issues involved in embedded system development using real time operating systems.	Analyze	PO1,PO2 (L2,L3)
CO3	**Relate** the recent trends and overview in the Design of Embedded systems.	Evaluate	PO3 (L2)
CO4	**Develop** an embedded systems applications for a given specification using high level and assembly level language.	Create	PO3(L3)

Text Book(s):

1. **"Introduction to Embedded Systems"** Shibu K V, Second edition, Tata McGraw Hill Education Private Limited, 2009, 2nd Edition, ISBN (13): 978-0-07-014589-4.

Reference Book(s):

1. **"Embedded Systems – A Contemporary Design Tool**" James K Peckol, John Weily, 2008.
2. **"Embedded Systems Design: An Introduction to Processes, Tools, andTechniques "** by Arnold S. Berger ISBN: 1578200733 CMP Books © 2002

Web and Video link(s):

1. https://www.edx.org/learn/embedded-systems
2. https://www.youtube.com/watch?v=KfFBEBN5UHU

E-Books/Resources:

1. https://www.electronicsforu.com/special/cool-stuff-misc/eight-free-ebooks-embedded-systems
2. https://link.springer.com/book/10.1007/978-3-030-60910-8

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2	2	3											2	3
#3			2											
#4			3											

Introduction to Image Processing

[As per Choice Based Credit System (CBCS) & OBE Scheme]

SEMESTER – VI

Course Code:	**P21EC6053**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. Understand the fundamentals of digital image processing
2. Understand the image enhancement techniques used in digital image processing
3. Understand the image restoration techniques and methods used in digital image processing
4. Understand the Morphological Operations and Segmentation used in digital image processing

UNIT – I	**8 Hours**

Digital Image Fundamentals: What is Digital Image Processing?, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sampling and Quantization.
Text 1: 1.1, 1.4, 1.5, 2.1, 2.2, 2.4

Self-study component:	Prepare a report on basic relationships between pixels of an image

UNIT – II	**8 Hours**

Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing.
Text 1: 3.1-3.3

Self-study component:	Comprehend the local Histogram Processing techniques

UNIT – III	**8 Hours**

Spatial Filters: Fundamentals of Spatial Filtering, Smoothing Spatial Filters.
Restoration: A model of the image Degradation/Restoration Process, Noise models.
Text 1: 3.4 - 3.5, 5.1- 5.2

Self-study component:	Develop an algorithm to add various intensity levels of salt and pepper noise to an image and remove.

UNIT – IV	**8 Hours**

Segmentation: Fundamentals, Point, Line, and Edge Detection, Thresholding, Region Based Segmentation.
A case study on impulse noise and Morphological Image Processing. (Refer, Ref1 and Ref2)
Text 1: 10.1, 10.2.1 - 10.2.5, 10.3-10.3.2, 10.4.

Self-study component:	Develop an algorithm to show dilation and erosion of an image.

UNIT – V	**8 Hours**

Morphological Image Processing: Preliminaries, Erosion and Dilation, Opening and Closing, the Hit-or-Miss Transforms, Some Basic Morphological Algorithms.
Color Image Processing: Color Fundamentals, Color Models.
A case study on Enhancement of Images using image processing methods.(Refer: Ref-3).
Text 1:9.5.1, 9.5.5, 9.5.6, 6.1-6.2.

Self-study component:	Develop an algorithm to convert colors of an image from RGB to HIS and vice versa.

Course Outcomes: On completion of this course, students are able to:			
COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	Apply basic mathematical and signal processing knowledge to understand different image processing stages/components.	Apply	**PO1[L1]**
CO2	Examine various types of images, intensity transformations and spatial filtering.	Analyse	**PO2[L2]**
CO3	Evaluate the techniques for image enhancement, segmentation and image restoration in the spatial domain.	Evaluate	**PO3[L2]**
CO4	Identify the different causes for image degradation and overview of image restoration techniques.	Understand	**PO1 [L2]**
CO5	Analyze the different feature extraction techniques for image analysis and recognition.	Analyse	**PO2 [L4]**

Text Book(s):

1. **Digital Image Processing-** Rafael C Gonzalez and Richard E. Woods, PHI 3rd Edition 2010.
   Ref-1: A Case Study of Impulse Noise Reduction Using Morphological Image Processing with Structuring Elements by V. Elamara et.al., Asian Journal of Scientific Research / DOI: 10.3923/ ajsr.2015.291.303
   Ref-2: Image Analysis Using Mathematical Morphology by Robert M. Haralicket. al., IEEE Transactions on Pattern Analysis and Machine Intelligence, Volume: PAMI-9, Issue: 4, July 1987, DOI: 10.1109/TPAMI.1987.4767941.
   Ref-3: Enhancement of Images using Morphological Transformations by K.Sreedhar and B.Panlal International Journal of Computer Science & Information Technology (IJCSIT) Vol 4, No 1, Feb 2012.

Reference Book(s):

1. **Digital Image Processing**- S.Jayaraman, S.Esakkirajan, T.Veerakumar, TataMcGraw Hill 2014.
2. **Fundamentals of Digital Image Processing**-A. K. Jain, Pearson 2004.

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2		2												2
#3			2											
#4	2												2	
#5		3												3

Automotive Electronics
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – VI

Course Code:	**P21EC6054**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**3:0:0**	**CIE Marks:**	**50**
Total Theory Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students to:

1. To understand the concepts of Automotive Electronics and its evolution and trends.
2. To learn and understand the various application of electronics systems and ECU in automotive.
3. To learn and understand principles and applications of sensors and actuators in automotive electronics systems.
4. To learn and understand various control systems in automotive.
5. To learn and understand the various communication protocols in automotive.
6. To learn and understand the modern advanced technologies and trends in automotive.

UNIT – I **8 Hours**

Architecture: - Overview, Vehicle system architecture.
Electronic control unit: - Operating conditions, Design, Data processing, Digital modules in the control unit Control unit software, Software Development**.**
Text 1

Self-study component:	1. Study of Basic fundamental of Automotive. 2. Study of Automotive Networking in different Application.

UNIT – II **8 Hours**

Basic principles of networking: - Network topology, Network organization, OSI reference model, Control mechanisms.
Automotive networking: -Cross-system functions, Requirements for bus systems, Classification of bus systems, Applications in the vehicle, Coupling of networks, Examples of networked vehicles.
Bus systems: - Controller Area Network.
Text 1

Self-study component:	1. Study of Basic working of electronic engine 2. Comparative study of different types of electronic ignition.

UNIT – III **8 Hours**

Bus systems: - LIN bus, Bluetooth, MOST bus, TTP/C, Flex Ray, Diagnosis interfaces.
Automotive sensors: - Basics and overview, Automotive applications, Features of vehicle sensors, Sensor classification, Main requirements, trends, Overview of the physical effects for sensors, Overview and selection of sensor technologies.
Vehicle security systems: -Acoustic signaling devices, Central locking system, Locking systems, Biometric systems
Text 1

Self-study component:	1. Angular Rate Sensor and Flex-Fuel Sensor. 2. Automotive Engine Control Actuators.

UNIT – IV **8 Hours**

Electronic Transmission Control: -Drive train Management, Market Trends, Control of Automated Shift Transmission AST, Control of Automatic Transmissions, Control of Continuously Variable Transmission, ECUs for Electronic Transmission Control, Thermo-Management, Processes and Tools Used in ECU Development.

Antilock Braking System (ABS): - System overview, Requirements placed on ABS, Dynamics of a braked wheel, ABS control loop, Typical control cycles.
Text 1

Self-study component:	1. Study ofDesign Engine control system. 2. Study of Program control units.

UNIT – V **8 Hours**

Electronic Diesel Control (EDC): - System overview, Common-rail system for passenger cars, Common-rail system for commercial vehicles, Data processing, Fuel-injection control, Lambda closed-loop control for passenger-car diesel engines, Torque-controlled EDC systems, Data exchange with other systems, Serial data transmission (CAN)
Automatic brake functions, Sensotronic brake control (SBC): -Overview. Standard function. Additional functions, Purpose and function, Design, Method of operation.
Active steering: -Purpose, Design, Method of operation, Safety concept, Benefits of active steering for the driver.
Text 1

Self-study component:	1. Study of Electronic Control System Diagnostics. 2. Study of Lane Departure Monitor and Tyre Pressure Monitoring System.

Course Outcomes: On completion of this course, students are able to:

COs	**Course Outcomes** with ***Action verbs*** for the Course topics	**Bloom's Taxonomy Level**	**Program Outcome Addressed (PO #) with BTL**
CO1	**Understand** an overview of automotive components, subsystems, and basics of Electronic Engine Control in today's automotive industry	Understand and Apply	PO1(L2)
CO2	**Apply** available automotive sensors and actuators in various electronic control systems while designing automotive system design	Apply	PO1(L3)
CO3	**Analyze** the networking of various modules in automotive systems and communication protocols of interfacing different electronics components, systems and mechanical counterparts.	Analyze	PO1(L2), PO2(L3)
CO4	**Analyze** the different automotive control systems and Safety-Related Systems	Analyze	PO1(L2), PO2(L3)

Text Book(s):
1. **Automotive Mechatronics Automotive Networking, Driving Stability Systems, Electronics. Spingervieweg.** ISBN 978-3-658-03974-5 ISBN 978-3-658-03975-2(eBook) DOI 10.1007/978-3-658-03975-2 Library of Congress Control Number: 2014946887

Reference Book(s):
1. Automotive Electronics Design Fundamentals – NazamuzZaman, 2015, Springer Publications.ISBN: 978-3-319-17584-3.

Web and Video link(s):
1. Automotive Electronics- https://youtu.be/BOP8qLQzhDc
2. Fundamentals of Automotive System-https://youtu.be/hs7bABMtOMI.
3. Electric Vehicles – Design & Development-https://youtu.be/zzpOtJA-Rqw

E-Books/Resources:

1. https://www.elsevier.com/books/understanding-automotive-electronics/ribbens/978-0-12-810434-7
2. https://www.academia.edu/42742205/Bosch_Professional_Automotive_Information

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	2												2	
#2	3												3	
#3	2	3											2	3
#4	2	3											2	3

Analog and Digital VLSI Design Laboratory
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – VI

Course Code:	**P21ECL606**	**Credits:**	**01**
Teaching Hours/Week (L:T:P):	**0-0-2**	**CIE Marks:**	**50**
Contact Period:	**Lab: 2 Hrs., Exam: 2 Hrs.**	**SEE Marks:**	**50**

A. Course Learning Objectives (CLOs)

This course aims to:

1. Explore the CAD tool and understand the flow of the Full Custom IC design cycle.
2. Learn DRC, LVS and Parasitic Extraction of the various designs.
3. Design and simulate the various basic CMOS analog circuits and use them in higher circuits like operational amplifiers using design abstraction concepts.
4. Design and simulate the various basic CMOS digital circuits and use them in higher circuits like adders and shift registers using design abstraction concepts
5. Understand simulation and synthesis of digital design.
6. Analyze the ASIC Design flow.
7. RTL Design, simulate and verify digital circuits

Course Content

Part A: Digital VLSI Design

ASIC-Digital Design / FPGA Digital Design:
the following experiments involve synthesis and verification for logical equivalence.

1. Develop Verilog Code for ALU.
2. Develop Verilog code for Universal Shift Register.
3. Develop Verilog Code for Serial adder.
4. Develop Verilog Code for Radix-4 Booth Multiplier.
5. Develop Verilog Code for Parallel adder.
6. Develop Verilog code for State Machine.

Part B. Analog VLSI Design

Analog Design Flow:

Perform the following steps for experiments listed below:

Steeps

1. Draw the schematic and verify the following: DC Analysis, Transient Analysis.
2. Draw the Layout and verify the DRC, ERC, and check for LVS.
3. RC extraction

Experiments

1. Design a NAND and NOR gate with given specification.
2. Design the following amplifiers in different topologies, for the given specification
   - Common source amplifier
   - Common Drain amplifier.
3. Design an OPAMP for given specifications using Differential Amplifier.

Open Ended Experiments:

1. Design and simulate Gilbert cell for Analog multiplication

Course Outcomes

CO #	Course Outcome	Bloom's Taxonomy Level	Level indicator Program Outcome
CO1	**Apply** the knowledge of the digital system to design of the schematic and layout in cadence tools.		**PO1 (L1)**
CO2	**Interpret** the outcome of DC Analysis, AC Analysis and Transient Analysis in analog circuits.		**PO4, PO9 (L4)**
CO3	**Design** and **simulate** basic CMOS circuits like inverter, common source amplifier and differential amplifiers.		**PO3, PO5, PO8,(L5)**
CO4	**Analysis** of the **design** for power, timing and area.		**PO2, PO5 (L4)**
CO5	**Develop** 4/8-bit Carry Ripple Adder, Carry Look Ahead adder and Booth Multiplication using Verilog code.		**PO3, PO5, PO7, (L5)**

Course Articulation Matrix (CAM)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
#1	3												3	
#2				2					3					
#3			2		3			2						
#4		3			3									3
#5			2		3		2							

Mini Project
[As per Choice Based Credit System (CBCS) & OBE Scheme]
SEMESTER – VI

Course Code:	**P21EC607**	**Credits:**	**03**
Teaching Hours/Week (L:T:P):	**0 : 0 : 3**	**CIE Marks:**	**50**
Total Number of Teaching Hours:	**40**	**SEE Marks:**	**50**

Course Learning Objectives: This course will enable the students:

- To identify, discuss and justify the technical aspects of the chosen project with a comprehensive and systematic approach.
- To practice acquired knowledge within the chosen area of technology for project development.
- To reproduce, improve and refine technical aspects for engineering projects.
- To work as an individual or in a team in development of technical projects.
- To communicate and report effectively project related activities and findings.

Course Outcomes: On completion of this course, students are able to:

COs	Course Outcomes with *Action verbs* for the Course topics	Bloom's Taxonomy Level	Program Outcome Addressed (PO #) with BTL
CO1	**Apply** the knowledge to identify, gather information and analyze to formulate the problem definition for project through detailed investigation.	L3	PO1, PO2, PO4 (L3)
CO2	**Design** and formulate the solutions to real-world problems by applying the fundamental concepts of electronics learnt from previous and current semesters.	L4	PO2, PO3, PO6(L4)
CO3	**Select** the open source tools and resources in solving the problems.	L2	PO5(L2)
CO4	**Adapt** effective communication by presentation of the work with professional ethics as an individual or a member of a team	L2	PO8, PO9, P10 (L2)
CO5	**Develop** sustainable system with scope for enhancement and continue life-long learning**.**	L5	PO12(L3)

Course Articulation Matrix (CAM)

CO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS O1	PS O2
# 1	**3**	**3**		**2**									**3**	**3**
# 2		**2**	**3**			**1**								**2**
# 3					**3**									
# 4								**3**	**2**	**3**				
# 5												**3**		

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